MICROCYBER

HT5700
Low Power HART Modem

User Manual

CONTENT

1 Overview

HT5700 is a single-chip HART communication solution designed for use with HART®FSK half duplex modem, compliant with the HART physical layer specification requirements. The HT5700 integrates necessary filtering, signal detection, modulation, demodulation, and signal generation functions, requiring very few external components. At the same time, the chip also integrates a 0.5% precision oscillator, which can greatly save circuit board space and is an ideal choice for designing HART circuits.

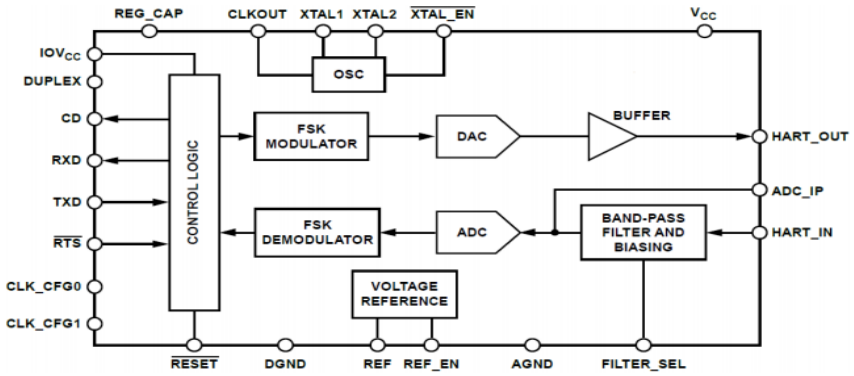

Figure 1 Function Block Diagram

1.1 Features

- HART-compliant fully integrated FSK modem
- 115μA maximum supply current in receive mode
- Suitable for intrinsically safe applications
- Integrated receive band-pass filter-Minimal external components required
- Clocking optimized for various system configurations-Ultralow power crystal oscillator (60μA maximum), external CMOS clock source, precision internal oscillator
- Buffered HART output—extra drive capability
- 8kV HBM ESD rating
- 2.7V to 5.5V power supply
- 1.71V to 5.5V interface
- -40°C to +125°C operation
- 4mm × 4mm QFN package
- HART physical layer compliant
- UART interface

1.2 Applications

- Field transmitters
- HART multiplexers
- PLC and DCS analog I/O modules
- HART network connectivity

2 Specifications

2.1 Specifications

VCC =2.7V to 5.5V, IOVCC = 1.71V to 5.5V, AGND = DGND, CLKOUT disabled, HART_OUT with 5nF load, internal and external receive filter, internal reference; all specifications are from −40°C to +125°C， unless otherwise noted.

Table 1 Specs sheet

Parameter ①	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS ②					
VCC	2.7		5.5	V	
IOVCC	1.71		5.5	V	
VCC and IOVCC Current Consumption					
Demodulator		86	115	µA	External clock, −40°C to +85°C
			179	µA	External clock, −40°C to +125°C
		69	97	µA	External clock, −40°C to +85°C, External reference
			157	µA	External clock, −40°C to +125 °C, External reference
Modulator		124	140	µA	External clock, −40°C to +85°C
			193	µA	External clock, −40°C to +125°C
		73	96	µA	External clock, −40°C to +85°C, External reference
			153	µA	External clock, −40°C to +125°C, External reference
Crystal Oscillator ③		33	60	µA	External crystal, 16 pF at XTAL1 and XTAL2
		44	71	µA	External crystal, 36 pF at XTAL1 and XTAL2
Internal Oscillator ④		87	110	µA	External crystal not required
Power-Down Mode					RESET=REF_EN= DGND
		30	45	µA	Internal reference disabled, −40°C to +85°C
			55	µA	Internal reference disabled, −40°C to +125°C
INTERNAL VOLTAGE REFERENCE					
Internal Reference Voltage	1.49	1.5	1.51	V	REF_EN= IOVCC to enable use of internal reference; VCC= 2.7V minimum
Load Regulation		18		ppm/µA	Tested with 50 µA load
OPTIONAL EXTERNAL VOLTAGE					
REFERENCE					
External Reference Input Voltage	2.47	2.5	2.53	V	REF_EN= DGND to enable use of external reference, VCC = 2.7V minimum
External Reference Input Current					
Demodulator		14	16	µA	Current required by external reference in receive mode
Modulator		37	40	µA	Current required by external reference in transmit mode
Internal Oscillator		14	16	µA	Current required by external reference if using internal oscillator
Power-Down		14	16	µA	
DIGITAL INPUTS					
VIH，Input High Voltage	0.7× IOVCC			V	
VIL，Input Low Voltage			0.3×OVCC	V	
Input Current	−0.1		+0.1	µA	
Input Capacitance ⑤		5		pF	Per pin

DIGITAL OUTPUTS					
VOH，Output High Voltage	IOVCC−0.5			V	
VOL，Output Low Voltage			0.4	V	
CD Assert ⑥	85	100	110	mVp-p	
HART_IN INPUT ⑤					
Input Voltage range	0		REF	V	External reference source
	0		1.5	V	Internal reference enabled
HART_OUT OUTPUT					
Output Voltage	459	493	505	mVp-p	AC-coupled (2.2µF), measured at HART_OUT pin with 160Ω load (worst-case load)
Mark Frequency ⑦		1200		Hz	Internal oscillator
Space Frequency ⑦		2200		Hz	Internal oscillator
Frequency Error	−0.5		+0.5	%	Internal oscillator, −40°C to +85°C
	−1		+1	%	Internal oscillator, −40°C to +125°C
Phase Continuity Error ⑤			0	Degrees	
Maximum Load Current ⑤		160		Ω	Worst-case load is 160Ω, ac-coupled with 2.2µF. for recommended configuration if driving a resistive load
Transmit Impedance		7		Ω	RTS low, at the HART_OUT pin
		70		kΩ	RTS high, at the HART_OUT pin
INTERNAL OSCILLATOR					
Frequency	1.2226	1.2288	1.2349	MHz	−40°C to+85°C
	1.2165	1.2288	1.2411	MHz	−40°C to+125°C
EXTERNAL CLOCK					
External Clock Source Frequency	3.6496	3.6864	3.7232	MHz	

① Temperature range: −40°C to +125°C; typical at 25°C.

② Current consumption specifications are based on mean current values.

③ The demodulator and modulator currents are specified using an external clock. If using an external crystal oscillator, the crystal oscillator current specification must be added to the corresponding VCC and IOVCC demodulator/modulator current specification to obtain the total supply current required in this mode.

④ The demodulator and modulator currents are specified using an external clock. If using the internal oscillator, the internal oscillator current specification must be added to the corresponding VCC and IOVCC demodulator/modulator current specification to obtain the total supply current required in this mode.

⑤ Guaranteed by design and characterization, but not production tested.

⑥ Specification set assuming a sinusoidal input signal containing preamble characters at the input and an ideal external filter (see Figure 18).

⑦ If the internal oscillator is not used, frequency accuracy is dependent on the accuracy of the crystal or clock source used.

2.2 Timing characteristics

VCC= 1.71V to 5.5V，IOVCC= 1.71V to 5.5V，T MIN to T MAX, unless otherwise noted.

Table 2 Timing characteristic sheet

Parameter	Limit at T MIN、T MAX	Unit	Description
t1	1	Bit time ①	Carrier start time. Time from RTS falling edge to carrier reaching its first peak.

t2	1	Bit time② max	Carrier stop time. Time from RTS rising edge to carrier amplitude dropping below the minimum receive amplitude.
t3	1	Bit time② max	Carrier decay time. Time from RTS rising edge to carrier amplitude dropping to ac zero.
t4	6	Bit time② max	Carrier detect on. Time from carrier on to CD rising edge.
t5	6	Bit time② max	Carrier detect off. Time from carrier off to CD falling edge.
t6	10	Bit time② max	Carrier detect on when switching from transmit mode to receive mode in the presence of a constant valid carrier. Time from RTS rising edge to CD rising edge.
t7	2.1	ms typ	Crystal oscillator power-up time. On application of a valid power supply voltage at VCC or on enabling of the oscillator via the XTAL_EN pin. Crystal load capacitors = 16pF.
t8	6	ms typ	Crystal oscillator power-up time. Crystal load capacitors = 36pF.
t9	25	μs typ	Internal oscillator power-up time. On application of a valid power supply voltage at VCC or on enabling of the oscillator via the CLK_CFG0 and CLK_CFG1 pins.
t10	10	ms typ	Reference power-up time.
t11	30	μs typ	Transition time from power-down mode to normal operating mode (external clock source, external reference).

① Specifications apply to HT5700 configured with internal or external receive filter.

② Bit time is the length of time to transfer one bit of data (1 bit time = 1/1200Hz = 833.333μs).

2.3 Absolute maximum ratings

TA=25°C, unless otherwise noted.

Table 3 Rated parameter table

Parameter	Rating
VCC to GND	- 0.3V to +7V
IOVCC to GND	- 0.3V to +7V
Digital Inputs to DGND	- 0.3V to IOVCC + 0.3V or +7V (whichever is less)
Digital Output to DGND	- 0.3V to IOVCC + 0.3V or +7V (whichever is less)
HART_OUT to AGND	- 0.3V to+2.5V
HART_IN to AGND	- 0.3V to IOVCC + 0.3V or +7V (whichever is less)
ADC_IP	- 0.3V to IOVCC + 0.3V or +7V (whichever is less)
AGND to DGND	- 0.3V to+0.3V
Operating Temperature Range（TA）Industrial	-40° C to+125°C
Storage Temperature Range	-65° C to+150°C
Junction Temperature（TJ MAX）	150°C
Power Dissipation	(TJ MAX-TA)/θJA
ESD	
Human Body Model	8 kV
Field Induced Charge Model	1.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum

operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ JA is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface -mount packages.

Table 4 Thermal Resistance

Package Type	θ JA ①	θ JC	Unit
24-Lead QFN	56	3	°C/W

① Thermal impedance simulated values are based on JEDEC 2S2P thermal test.

3 PIN Configuration And Function Descriptions

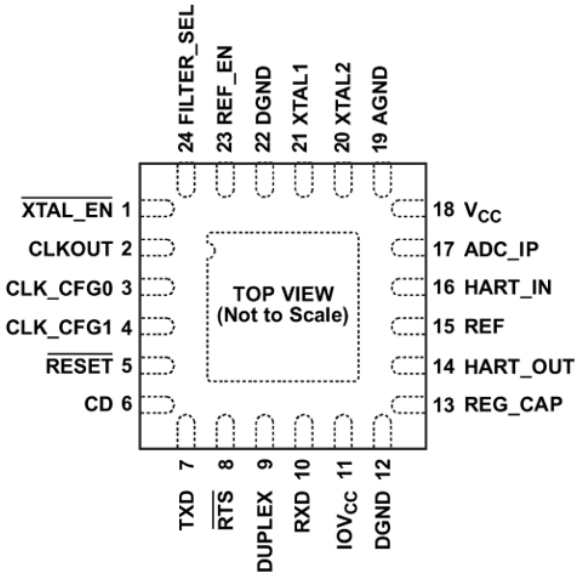

Figure 2 Pin Configuration

Table 5 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	XTAL_EN	Crystal Oscillator Circuit Enable. A low state enables the crystal oscillator circuit, and an external crystal is required. A high state disables the crystal oscillator circuit, and an external clock source or the internal oscillator provides the clock source. This pin is used in conjunction with the CLK_CFG0 and CLK_CFG1 pins in configuring the required clock generation scheme.
2	CLKOUT	Clock Output. If using the crystal oscillator or the internal RC oscillator, a clock output can be configured at the CLKOUT pin. Enabling the clock output consumes extra current to drive the load on this pin. See the CLKOUT section for more details.
3	CLK_CFG0	Clock Configuration Control. See Table 6.
4	CLK_CFG1	Clock Configuration Control. See Table 6.
5	RESET	Active Low Digital Input. Holding $\overline{\text{RESET}}$ low places the HT5700 in power-down mode. A high state on $\overline{\text{RESET}}$ returns the HT5700 to their power-on state. If not using this pin, tie this pinto IOVCC.
6	CD	Carrier Detect—Digital Output. A high on CD indicates a valid carrier is detected.
7	TXD	Transmit Data—Digital Input. Data input to the modulator.
8	RTS	Request to Send—Digital Input. A high state enables the demodulator and disables the modulator. A low state enables the modulator and disables the demodulator.
9	DUPLEX	A high state on this pin enables full duplex operation. See the Theory of Operation section. A low state disables this feature.
10	RXD	Receive Data—UART Interface Digital Data Output. Data output from the demodulator is accessed on this pin.
11	IOVCC	Digital Interface Supply. Digital threshold levels are referenced to the voltage applied to this pin. The applied voltage can be in the range of 1.71V to 5.5 V. IOVCC should be decoupled to ground with low ESR 10μF and 0.1μF capacitors (see the Supply Decoupling section).
12	DGND	Digital Circuitry Ground Reference Connection. For typical operation, it is recommended to connect this pin to AGND.
13	REG_CAP	Capacitor Connection for Internal Voltage Regulator. Connect a 1μF capacitor from this pinto ground.
14	HART_OUT	HART FSK Signal Output. See the FSK Modulator section and Figure 28 for typical connections.
15	REF	Internal Reference Voltage Output, or External 2.5V Reference Voltage Input. Connect a 1μF capacitor from this pinto ground. When supplying an external reference, the VCC supply requires a minimum voltage of 2.7 V.

16	HART_IN	HART FSK Signal. When using the internal filter, couple the HART input signal into this pin using a 2.2nF series capacitor. If using an external band-pass filter as shown in Figure 22, do not connect to this pin.
17	ADC_IP	If using the internal band-pass filter, connect 680 pF to this pin. Alternatively, this pin allows direct connection to the ADC input, in which case an external band-pass filter network must be used, as shown in Figure 21.
18	VCC	Power Supply Input. 2.7V to 5.5V can be applied to this pin. VCC should be decoupled to ground with low ESR 10μF and 0.1μF capacitors (see the Supply Decoupling section).
19	AGND	Analog Circuitry Ground Reference Connection.
20	XTAL2	Connection for External 3.64MHz Crystal. Do not connect to this pin if using the internal RC oscillator or an external clock source.
21	XTAL1	Connection for External 3.6864MHz Crystal or External Clock Source Input. Tie this pinto ground if using the internal RC oscillator.
22	DGND	Digital Circuitry Ground Reference Connection. For typical operation, it is recommended to connect this pin to AGND.
23	REF_EN	Reference Enable. A high state enables the internal 1.5V reference and buffer. A low state disables the internal reference and input buffer, and a buffered external 2.5V reference source must be applied at REF. If REF_EN is tied low, VCC must be greater than 2.7V.
24	FILTER_SEL	Band-Pass Filter Select. A high state enables the internal filter and the HART signal should be applied to the HART_IN pin. A low state disables the internal filter and an external band-pass filter must then be connected at the ADC_IP input pin. In this case, the HART signal should be applied to the ADC_IP pin.
EPAD	EPAD	The exposed paddle must be connected to AGND or DGND, or, alternatively, it can be left electrically unconnected. It is recommended that the paddle be thermally connected to a copper plane for enhanced thermal performance.

4 Typical Performance Characteristics

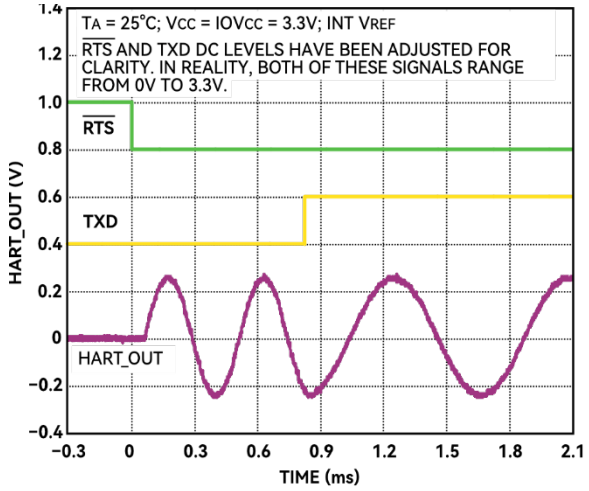

Figure 3 Carrier Startup Time

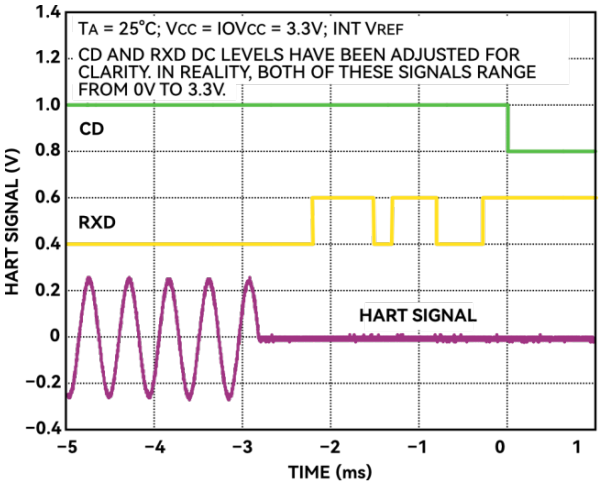

Figure 4 Carrier Detection Shutdown Time

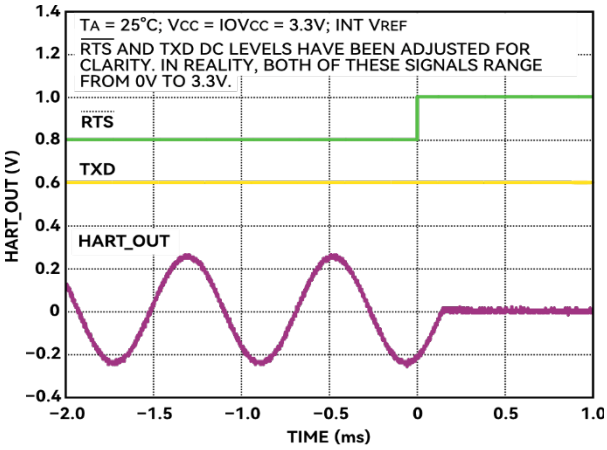

Figure 5 Carrier Stop/Decay Time

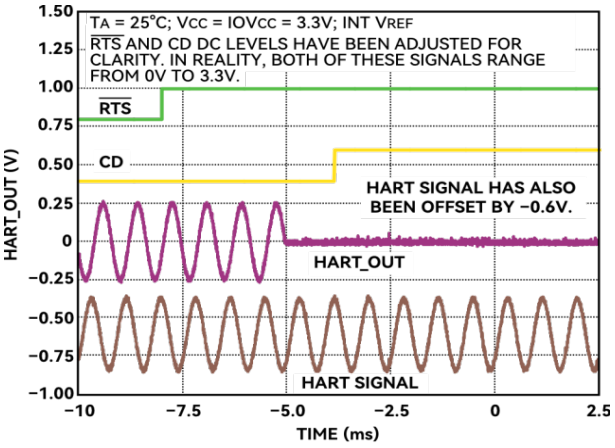

Figure 6 When switching from transmission mode to reception mode with a constant effective carrier, the timing for enabling carrier detection is determined.

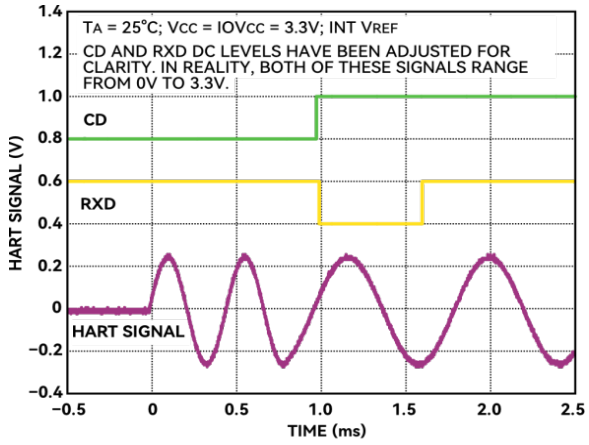

Figure 7 Carrier Detection Start Time

5 Theory of Operation

Highway Addressable Remote Transducer (HART) Communication is the global standard for sending and receiving digital information across analog wires between smart field devices and control systems. This is a digital two -way communication system, in which a 1mA p-p frequency shift keyed (FSK) signal is modulated on top of a 4mA to 20mA analog current signal. HT5700 are designed and specified to operate as a single -chip, low power, HART FSK half-duplex modem, complying with the HART physical layer requirements .

The HT5700 not only integrate the modulation and demodulation functions, but also contain an internal reference, an integrated receive band-pass filter (which has the flexibility of being bypassed if required), and an internally buffered HART output, giving a high output drive capability and removing the need for external buffering. The HT5700 also contains a precision internal RC oscillator. As a result of such extensive integration options, minimal external components are required.

The HT5700 either transmit or receive 1.2kHz and 2.2kHz carrier signals. A 1.2kHz signal represents a digital 1, or mark, whereas a 2.2kHz signal represents a 0, or space. There are three main clocking configurations supported by these parts: External crystal, CMOS clock input, Internal RC oscillator.

The device is controlled via a standard UART interface. The relevant signals are RTS, CD, TXD, and RXD (see Table 6 for more detail on individual pin descriptions).

5.1 FSK Modulator

The modulator converts a bit stream of UART -encoded HART data at the TXD input to a sequence of 1200Hz and 2200Hz tones (see Figure 8). This sinusoidal signal is internally buffered and output on the HART_OUT pin.

The modulator is enabled by bringing the RTS signal low.

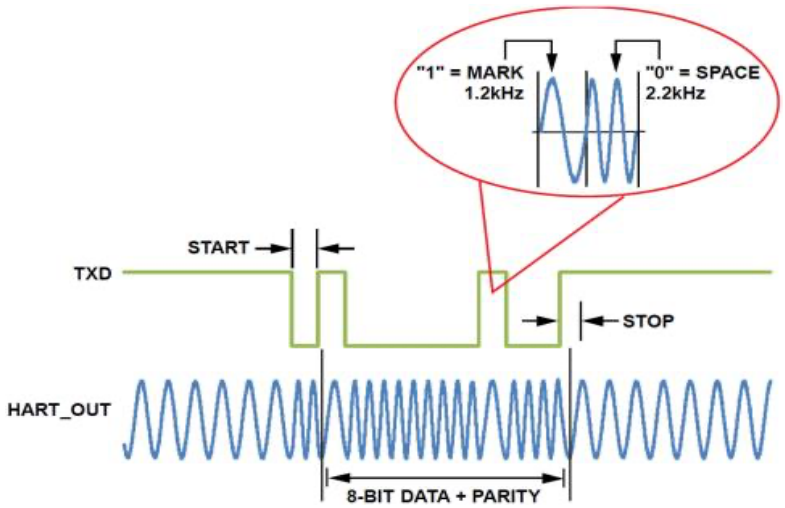

Figure 8 HT5700 Modulator Waveform

The modulator block contains a DDS engine that produces a 1.2kHz or 2.2kHz sine wave in digital form and then performs a digital-to-analog conversion. This DDS engine inherently generates continuous phase signals, thus avoiding any output discontinuity when switching between frequencies. Figure 9 demonstrates a simple implementation of this FSK encoding.

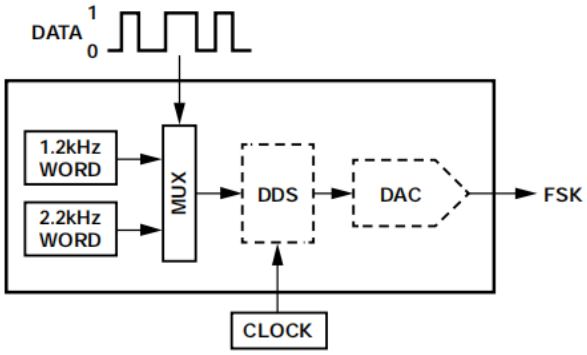

Figure 9 DDS-Based FSK Encoder

5.2 FSK Demodulator

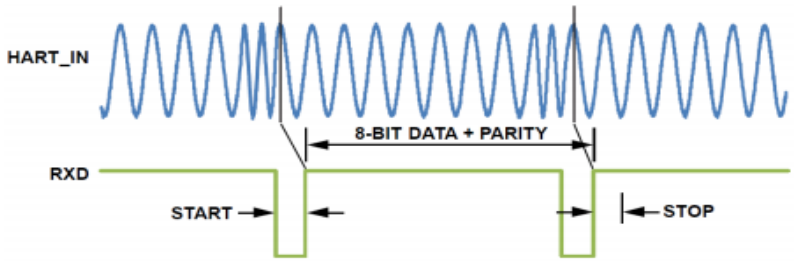

Figure 10 HT5700 Demodulator Waveform (Preamble Message 0xFF)

When HT5700 are in receive mode. A high on CD indicates a valid carrier is detected. The demodulator accepts an FSK signal at the HART_IN pin and restores the original modulated signal at the UART interface digital data output pin, RXD. The combination of the ADC, digital filtering and digital demodulation results in a highly accurate output on the RXD pin. The HART bit stream follows a standard UART frame with a start bit, 8 -bit data, one parity, and a stop bit (see Figure 20). RTS is logic high, the modulator is disabled and the demodulator is enabled.

5.3 Connecting to HART_IN or ADC_IP

The HT5700 have two filter configuration options: an external filter (HART signal is applied to ACP_IP) and an internal filter (HART signal is applied to HART_IN).

The external filter configuration is shown in Figure 11. In this case, the HART signal is applied to the ADC_IP pin through an external filter circuit. In safety critical applications, the HT5700 must be isolated from the high voltage of the loop supply. The recommended external band-pass filter includes a 150kΩ resistor, which limits current to a sufficiently low level to adhere to intrinsic safety requirements. In this case, the input has higher transient voltage protection and should, therefore, not require additional protection circuitry, even in the most demanding of industrial environments. Assuming the use of a 1% accurate resistor and 10% accurate capacitor components, the calculated variation in CD trip voltage levels vs. the ideal is ±3.5 mV.

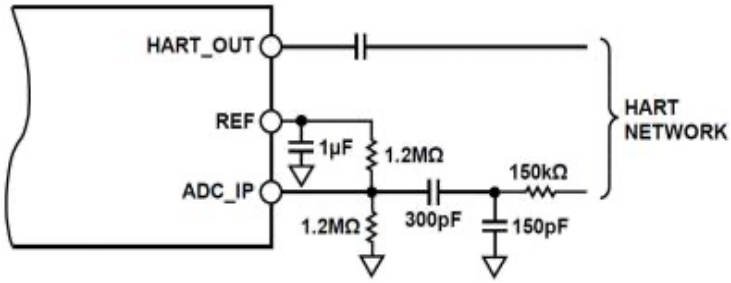

Figure 11 HT5700 with External Filter on ADC_IP

The internal filter configuration is shown in Figure 12. This option is beneficial where cost or board space is a large concern because it removes the need for multiple external components. This configuration achieves an 8 kV ESD HBM rating but requires extra external protection circuitry for EMC and surge protection purposes if used in harsh industrial environments.

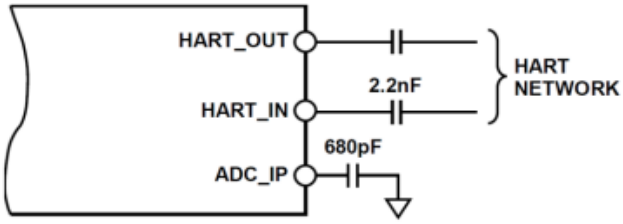

Figure 12 HT5700 Using Internal Filter on HART_IN

5.4 Clock Configuration

The HT5700 support numerous clocking configurations to allow the optimal trade -off between cost and power: External crystal, CMOS clock input, Internal RC oscillator.

The CLK_CFG0, CLK_CFG1, and XTAL_EN pins configure the clock generation as shown in Table 6. The HT5700 can also provide a clock output at CLKOUT (for more details, see the CLKOUT section).

5.4.1 External Crystal

The typical connection for an external crystal (ABLS-3.6864MHZ-L4Q-T) is shown in Figure 13. To ensure minimum current consumption and to minimize stray capacitances, connections between the crystal, capacitors, and ground should be made as close to the HT5700 as possible.

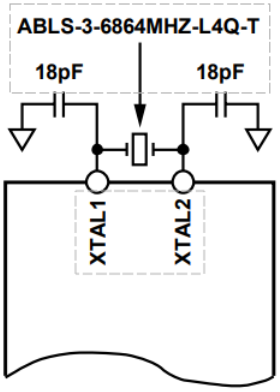

Figure 13 Crystal Oscillator Connection

ABLS-3.6864MHZ-L4Q-T crystal oscillator data sheet recommends using two 18pF capacitors.

5.4.2 CMOS Clock Input

A CMOS clock input can also be used to generate a clock for the HT5700. To use this mode, connect an external clock source to the XTAL 1 pin, and leave XTAL2 open circuit (see Figure 14).

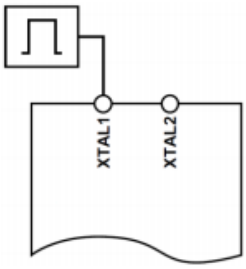

Figure 14 CMOS Clock Connection

5.4.3 Internal Oscillator

Consuming typically 87μA, the low power, internal, 0.5% precision RC oscillator has an oscillation frequency of 1.2288MHz. To use this mode, tie the XTAL1 pin to ground and leave the XTAL2 pin open circuit (see Figure 15).

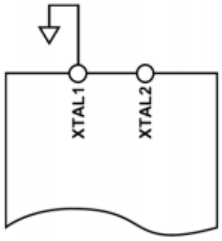

Figure 15 Internal Oscillator Connection

5.4.4 CLKOUT

The HT5700 can provide a clock output at CLKOUT (see Table 6)。

• If using the crystal oscillator, this clock output can be configured as a 3.6864MHz, 1.8432MHz, or. 1.2288MHz buffer clock.

• If using a CMOS clock, no clock output can be configured at the CLKOUT pin.

• If using the internal RC oscillator, this clock output is only available as a 1.2288MHz buffer clock.

The amplitude of the clock output depends on the IOVCC level; therefore, the clock output can be in the range of 1.71V p-p to 5.5V p-p. Enabling the clock output of the HT5700 increases the current consumption of the device. This increase is due to the current required to drive any load at the CLKOUT pin, which should not be more than 30pF.

This capacitance should be minimized to reduce current consumption and provide the clock with the cleanest edges. The additional current drawn from the IOVCC supply can be calculated using the following equation:

$I = C \times V \times f$

Table 6 Clock Configuration Options

XTAL_EN	CLK_CFG1	CLK_CFG0	CLKOUT	Description
1	0	0	No output	3.6864MHz CMOS clock connected at XTAL1 pin
1	0	1	No output	1.2288MHz CMOS clock connected at XTAL1 pin
1	1	0	No output	Internal oscillator enabled
1	1	1	1.2288MHz output	Internal oscillator enabled, CLKOUT enabled
0	0	0	No output	Crystal oscillator enabled
0	0	1	3.6864MHz output	Crystal oscillator enabled, CLKOUT enabled

0	1	0	1.8432MHz output	Crystal oscillator enabled, CLKOUT enabled
0	1	1	1.2288MHz output	Crystal oscillator enabled, CLKOUT enabled

5.4.5 POWER-DOWN Mode

The HT5700can be placed into power -down mode by holding the RESET pin low. If using the internal reference, it is recommended to tie the REF_EN pin to the RESET pin so that it is also powered down.

In this mode, the receive, transmit, and oscillator circuits are all switched off, and the device consumes a typical current of 30μA.

5.4.6 FULL DUPLEX Operation

Full duplex operation means that the modulator and demodulator of the HT5700 are enabled at the same time. This is a powerful feature, enabling a self-test procedure of not only the HART device but also the complete signal path between the HART device and the host controller. This provides verification that the local communications loop is functional. This increased level of system diagnostics is useful in production self-test and is advantageous in improving the application's safety integrity level (SIL) rating. The full duplex mode of operation is enabled by connecting the DUPLEX pin to logic high.

6 Applications Information

6.1 Supply Decoupling

It is recommended to decouple the VCC and IOVCC supplies with 10μF in parallel with 0.1μF capacitors to ground. For many applications, 1μF in parallel with 0.1μF ceramic capacitors to ground should be sufficient. The REG_CAP voltage of 1.8V is used to supply the HT5700 internal circuitry and is derived from the VCC supply using a high efficiency clocking LDO. Decouple this REG_CAP supply with a 1μF ceramic capacitor to ground. It is also required to decouple the REF pin with a 1μF ceramic capacitor to ground. Place decoupling capacitors as close to the relevant pins as possible.

For loop-powered applications, it is recommended to connect a resistance in series with the VCC supply to minimize the effect of any noise, which may, depending on the system configuration, be introduced onto the loop as a result of current draw variations from the HT5700. For typical applications, 470Ω of resistance has proven most effective. However, depending on the application conditions, alternative values may also be acceptable.

6.2 Transient Voltage Protection

Many industrial control applications have requirements for HART -enabled current input and output modules. Figure 26shows an example of a HART-enabled current input module that contains transient voltage protection circuitry, which is very important in harsh industrial control environments.

The module is powered from a 24V field supply, and the 250Ω load is within the low impedance module itself. This configuration is in contrast to Figure 17, which demonstrates a secondary HART device, in which the load is outside of the module. For transient voltage protection, a 10V unidirectional (for protection against positive high voltage transients) transient voltage suppressor (TVS) is placed at the connection point of the current input module. The TVS component that is used in a given application circuit must have power ratings that are appropriate to the individual system. When choosing the TVS, low leakage current is also an important specification for maintaining the accuracy of the analog current input. In the event of a transient spike, the 22Ω series resistor acts as a current limiting resistor for the FSK output pin. The FSK input pin is inherently protected by the 150kΩ resistor, which forms part of the recommended external filter circuitry at the FSK input. The voltage divider, made up of both a 75kΩ resistor and a 22kΩ resistor, is used to maintain a 0.75V dc bias at the field side of the FSK output switch.

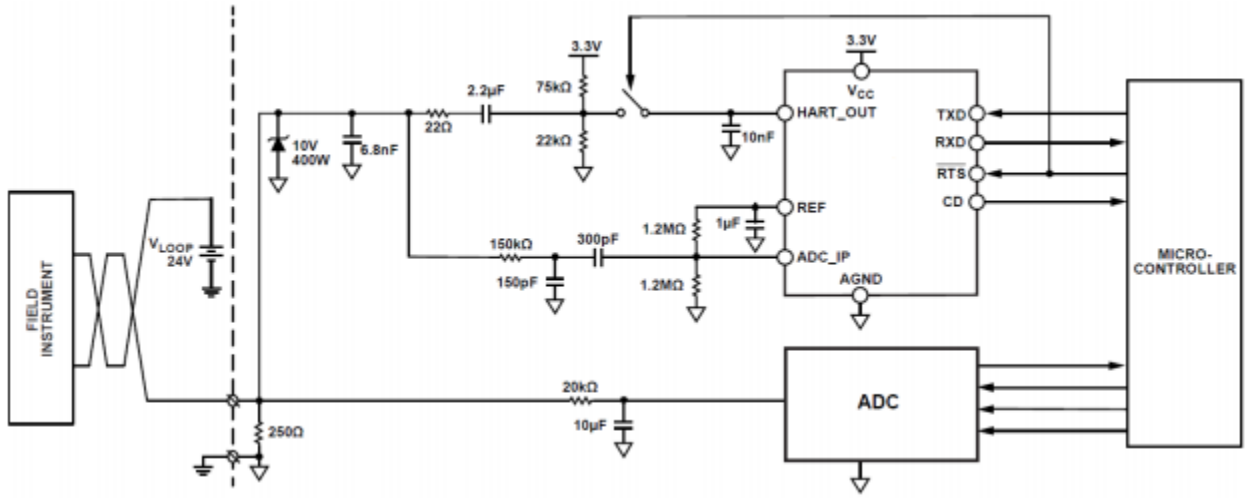

Figure 16 Current Input Module, HART Circuit

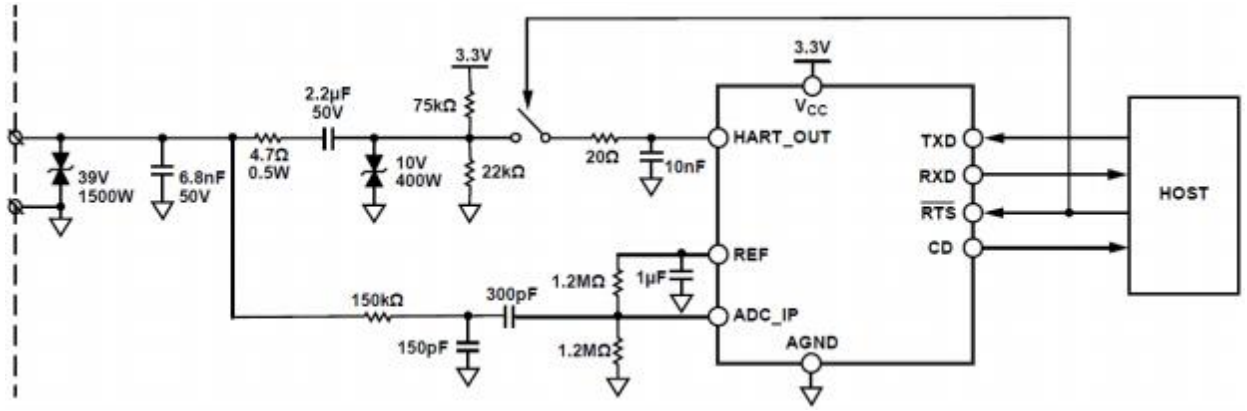

Figure 17 Secondary HART Device

As previously mentioned, Figure 17 shows an example secondary HART device, incorporating two-stage protection circuitry. In this example, a bidirectional (for protection against both positive and negative high voltage transients) TVS is included to provide flexibility in the polarity of the connection points of the module. Because this module could be connected to any point on the current loop, the higher TVS rating was chosen. The lower rated second stage provides added protection.

6.3 Typical Connection Diagrams

Figure 18 shows a typical connection diagram for the HT5700 using the external and internal options. See the Connecting to HART_IN or ADC_IP section for more details.

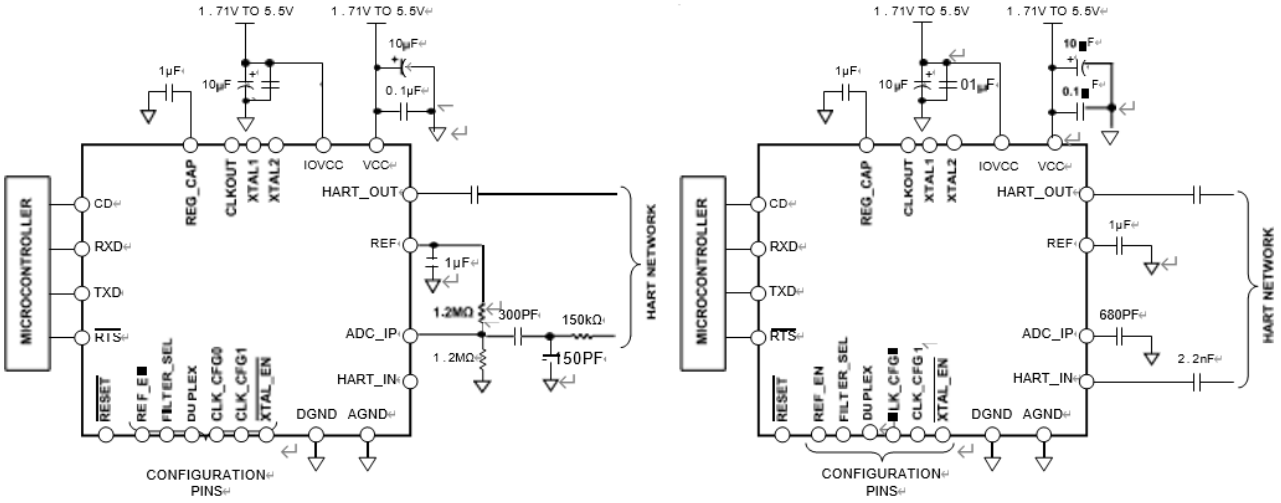

Figure 18 HT5700 Typical Connection Diagram for External and Internal Filter Options

Appendix 1 Outline Dimensions

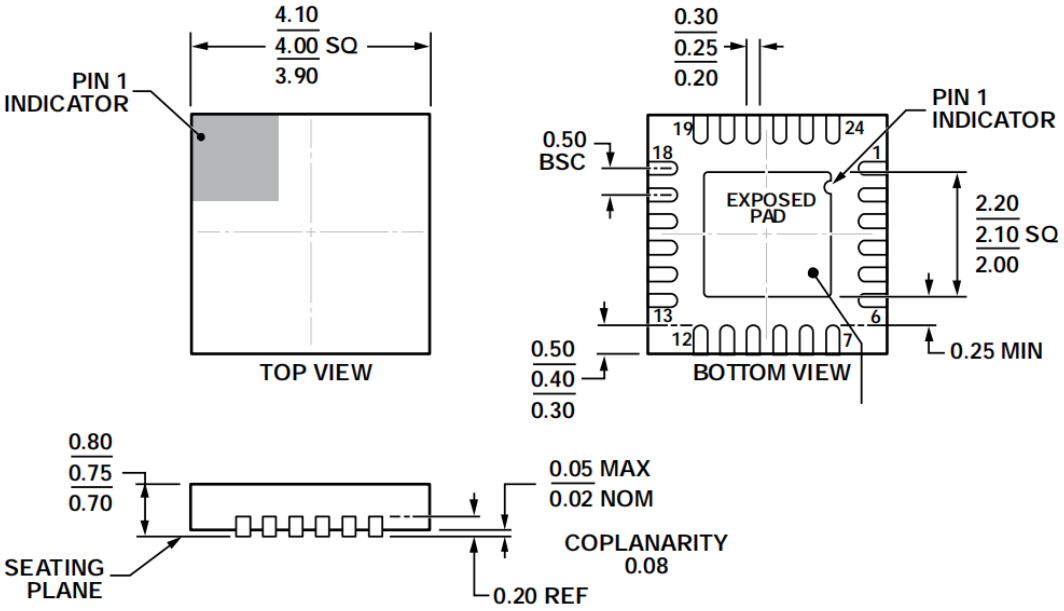

Figure 19 Package Description

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