MICROCYBER

APC3

DP Fieldbus Communication Controller

User Manual

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We have reviewed the contents of this publication to ensure consistency with the hardware and software described. Since variance cannot be precluded entirely, we cannot guarantee full consistency. However, the information in this publication is reviewed regularly and any necessary corrections are included in subsequent editions. Any suggestions for improvement are welcome.

Version：V2.2

Company Introduction

Microcyber Corporation established as a high-tech enterprise by the Shenyang Institute of Automation Chinese Academy of Sciences, mainly engages in advanced industrial control systems, equipments, instruments and chips for industrial process automation control solutions in the research, development, production and application. Microcyber undertakes a number of national scientific and technical key task and “863” project, and has Liaoning Province networked control systems engineering research center.

Microcyber successfully developed the first domestically certified fieldbus protocol master stack, the first nationally certified fieldbus instrument, and the first domestic safety instrument certified by German TüV, and co-hosted with other units It has formulated the first domestic industrial Ethernet protocol standard EPA and the first industrial wireless communication protocol standard WIA-PA, which have become IEC international standards.

The products and technologies of Microcyber have won two second prizes of National Science and Technology Progress Award, one National Science and Technology Invention Award, one first prize of Science and Technology Progress of Chinese Academy of Sciences, and one first prize of Liaoning Province Science and Technology Progress. The products are exported to Europe and the United States, etc. In developed countries, top companies in the industry such as Emerson in the United States, Rotork in the United Kingdom, and Bifold in the United Kingdom have adopted Microcyber 's key technologies or key components in their products, and have successfully completed more than 200 large-scale automation engineering projects.

Microcyber passed the Authentication of ISO 9001 Quality System, and has an outstanding innovative R&D team, plentiful practical experiences of design of the Automatic engineering, a leading product series, a huge market network, a strict quality management system and an excellent enterprise culture. All these further a solid foundation of entrepreneurship and sustainable development for Microcyber.

Carrying the ideals of employees, creating customer value and promoting enterprise development.

Contents

Chapter 1. Function Overview

APC3 is an ASICs chip for the development of PROFIBUS DP intelligent slave station. APC3 supports DPV0 in PROFIBUS DP standard.

Compatibility:

- Under 3.3V working voltage, it is fully compatible with VPC3 working in DPV0 mode

In addition to different working voltages, it is fully compatible with SPC3 working in DPV0 mode

Processor interface:

- Support Intel and Motorola processor interface modes; The interface mode can be configured through the XINT/MOT and MODE pins
- Users can directly operate internal dual port RAM through synchronous/asynchronous 8-bit data interface and 11 bit address bus

Clock:

- APC3 needs to provide 48MHZ external clock;
- APC3 can output 24M/12M clock to external processor

Software interface:

- APC3 integrates 1.5k dual port RAM, which is mainly used for the interface between APC3 and software;
- Dual port RAM is divided into 192 segments, each segment includes 8 bytes. The software's operation on dual port RAM is in segments

Status indication:

- MAC status in APC3 can be queried through the status register at any time, such as Offline/Passive idle, DP State WD-State, Baud rate status, etc;
- Various external events can be obtained through the interrupt request register to obtain relevant data, such as user extended parameter data, etc

Baud rate identification:

- APC3 can automatically identify the baud rate in the range of 9.6Kbps~12Mbps;
- Baud rate values are respectively: 12M, 6M, 3M, 1.5M, 500k, 187.5k, 93.75k, 45.45k, 19.2k, 9.6k, in bps

Temperature characteristics:

- Storage temperature: -65~150℃

- Working temperature: -40~85℃
- Junction temperature: -40~85℃

Chapter 2. Pin Description

2.1 Pin function definition

APC3 adopts 44 pin PQFP package, and the pin definition is shown in Table 2.1 below.

Table 2.1 Pin Function Definition

Pin	Signal Name	In/Out	Description		Source/Destination
1	XCS	I(C)	Chip-Select	C32 Mode : connect to VDD C165 Mode: CS-Signal	CPU (80C165)
2	XW R/E_CLOCK	I(C)	Write signal / E_Clock for Motorola		CPU
3	DIVIDER	I(C)	Setting the scaling Factor for CLKOUT2/4	'O' = CLK divided by 4 '1' = CLK divided by 2	
4	XRD/R_W	I(C)	Read Signal / Read _Write for Motorola		CPU
5	CLK	I(TS)	Clock pulse input		System
6	**VSS**				
7	CLKOUT2/4	O	Clock Output (System Clock divided by 2 or 4)		System, CPU
8	XINT/MOT	I(C)	'0' = Intel Interface '1' = Motorola Interface		Configuration Pin
9	X/INT	O	Interrupt		CPU; Interrupt-Controller
10	AB10	I(CPD)	Address bus	C32 Mode: '0' C165 Mode: Address Bus	System, CPU
11	DB0	I(C)/O	**Data Bus**	**C32 Mode: Data/Address Bus multiplexed** **C165 Mode: Data/Address Bus separated**	**CPU, Memory**
12	DB1	I(C)/O			
13	XDATAEXCH	O	Indicates DATA-EXCH state for PROFIBUS-DP		LED
14	XREADY/XDTACK	O	Ready for external CPU		System, CPU
15	DB2	I(C)/O	**Data Bus**	**C32 Mode: Data/Address Bus multiplexed** **C165 Mode: Data/Address Bus separated**	**CPU, Memory**
16	DB3	I(C)/O			
17	**VSS**				
18	**VDD**				
19	DB4	I(C)/O	**Data Bus**	**C32 Mode: Data/Address Bus multiplexed** **C165 Mode: Data/Address Bus separated**	**CPU, Memory**
20	DB5	I(C)/O			
21	DB6	I(C)/O			
22	DB7	I(C)/O			
23	MODE	I	'0' = 80C166 Data/Address Bus separated; Ready Signal '1' = 80C32 Data/Address Bus multiplexed, fixed Timing		Configuration Pin

24	ALE/AS	I(C)	Address latch enable	C32 mode: ALE C165 mode: <log> 0	CPU (80C32)
25	AB9	I	Address bus	C32 Mode: '0' C165 Mode: Address Bus	CPU (C165), memory
26	TXD	O	Serial send port		PROFIBUS Interface
27	RTS	O	Request to Send		PROFIBUS Interface
28	**VSS**				
29	AB8	I(C)	Address bus	C32 Mode: '0' C165 Mode: Address Bus	CPU (C165), memory
30	RXD	I(C)	Serial Receive Port		PROFIBUS Interface
31	AB7	I(C)	**Address bus**	**C32 Mode: '0'** **C165 Mode: Address Bus**	CPU (C165), memory
32	AB6	I(C)			
33	XCTS	I(C)	Clear to Send: 'O' = send enable		FSK Modem
34	XTEST0	I(C)	Pin must be connected to VDD.		
35	XTEST1	I(C)	Pin must be connected to VDD.		
36	RESET	I(CS)	Connect Reset Input with CPU's port pin.		
37	AB4	I(C)	Address bus	C32 Mode: '0' C165 Mode: Address Bus	CPU (C165), memory
38	**VSS**				
39	**VDD**				
40	AB3	I(C)	**Address bus**	**C32 Mode: '0'** **C165 Mode: Address Bus**	CPU (C165), memory
41	AB2	I(C)			
42	AB5	I(C)			
43	AB1	I(C)			
44	AB0	I(C)			

Notes:

- All signals beginning with 'X' indicate "active at low level".
- C32-Mode means ‘Synchronous Intel Mode’ and C165-Mode means ‘Asynchronous Intel Mode’.
- VDD = +3.3 V
- VSS = 0 V

Input Levels:

- I (C) : CMOS
- I (CS) : CMOS, Schmitt-Trigger
- I (CPD) : CMOS, pulldown
- I (TS) : TTL, Schmitt-Trigger

2.2 Definition of pin outgoing line

APC3 is packaged with 44 pin PQFP, as shown below.

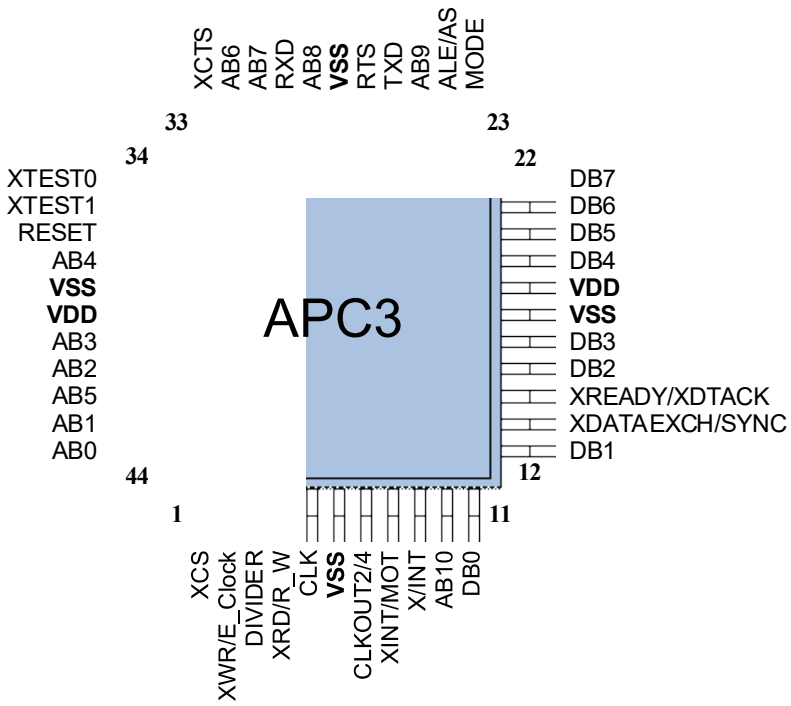

Figure 2.1 Definition of pin outgoing line

Chapter 3. Memory configuration

3.1 Memory Area Distribution in APC3

Figure 2.1Figure 3.1 shows the division diagram of 1.5k dual port RAM in APC3.

The APC3 internal latch/register is located at the first 21 addresses. The value of the internal latch/register either comes from APC3 or affects the APC3 controller. Specific units can only be read or written.

The APC3 organization parameter is located in the area with the starting address of 16H. The entire buffer structure (for DP-SAPs) is written based on these parameters. In addition, general parameter setting data (station address, Ident parameter, etc.) are stored in these units, and state parameters are also stored in these units (global control command, etc.).

The user generated buffer in APC3 is located in the area with the starting address of 40H. All buffer start addresses must start from the segment start address.

Table 3.1 APC3 memory area distribution

Address	Function	
000H	Processor parameters internal work cells Latches/register	internal work cells
016H	Organizational parameters (42 bytes)	
040H	DP- buffer: Data In (3) * Data Out (3) * Diagnostics (2) Parameter setting data (1) Configuration data (2)	

Note: HW cannot exceed the address range of 1.5k. That is, if the user writes or reads beyond the memory range

The address will subtract 400H, allowing the user to get a new address. This feature prevents overwriting the original process parameters. In this case, APC3 will generate a RAM access conflict interrupt. If the RAM access out of range is caused by an incorrect buffer initialization operation, the same error handling operation will be performed.

Note: Data In is the input data from the PROFIBUS slave station to the master station

Data Out is the output data from the PROFIBUS master station to the slave station

The dual port RAM in APC3 is logically divided into 192 fragments, each of which is composed of 8 bytes. See Figure 3.1.

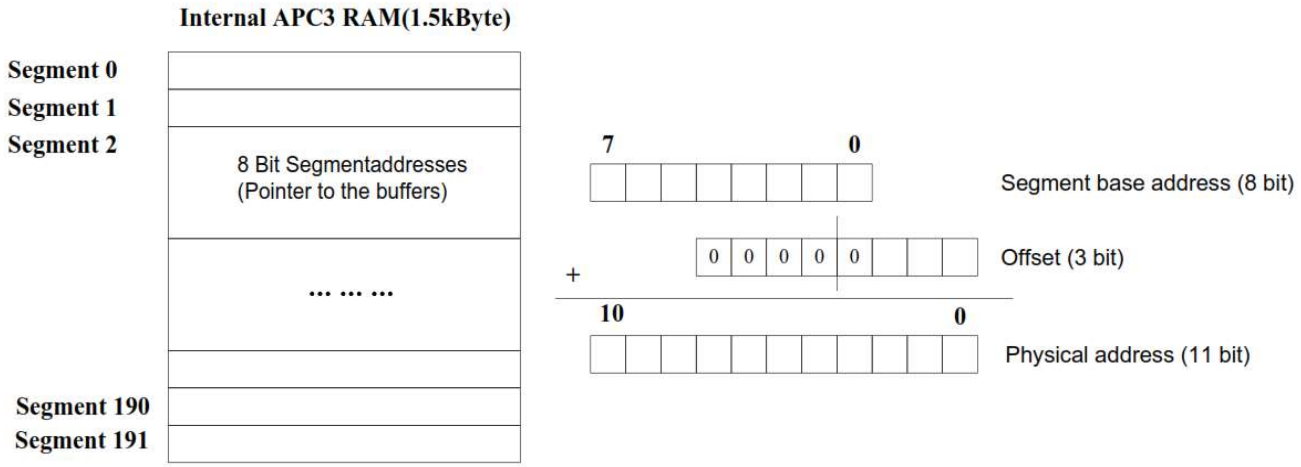

Figure 3.1 Schematic Diagram of APC3 Memory RAM Segmentation

3.2 Processor parameters

The cells in the address area 00H-07H support read-only or write only operations. The functional definitions of some units are different in Intel mode and Motorola mode, as shown in the following table.

Table 3.2 Internal parameter latch allocation under read operation

Address Intel / Motorola		Name	Bit No.	Significance (Read Access!)
00H	01H	Int-Req-Reg	7..0	Interrupt Controller Register
01H	00H	Int-Req-Reg	15..8	
02H	03H	Int−Reg	7..0	
03H	02H	Int−Reg	15..8	
04H	05H	Status-Reg	7..0	Status Register
05H	04H	Status-Reg	15..8	
06H	07H	Reserved		
07H	06H			
08H		Din_Buffer_SM	7..0	Buffer assignment of the DP_Din_Buffer_State_Machine
09H		New_Din_Buffer_Cmd	1..0	The user makes a new DP Din buffer available in the N state.
0AH		Dout_Buffer_SM	7..0	Buffer assignment of the DP_Dout_Buffer_State_Machine
0BH		Next_Dout_Buffer_Cmd	3..0	The user fetches the last DP Dout_Buf from the N state
0CH		Diag_Buffer_SM	3..0	Buffer assignment for the DP_Diag_Buffer_State_Machine
0DH		New_Diag_Buffer_Cmd	1..0	The user makes a new DP Diag Buffer available to the APC3.
0EH		User_Prm_Data_Okay	1..0	The user positively acknowledges the user parameter setting data of a Set_Param-Telegram.
0FH		User_Prm_Data_Not_Okay	1..0	The user negatively acknowledges the user parameter setting data of a Set_Param-Telegram.
10H		User_Cfg_Data_Okay	1..0	The user positively acknowledges the configuration data of a Check_Config-Telegram.
11H		User_Cfg_Data_Not_Okay	1..0	The user negatively acknowledges the configuration data of a Check_Config-Telegram.
12H		Reserved		
13H				
14H		SSA_Buffer_Free_Cmd		The user has fetched the data from the SSA buffer and enables the buffer again.
15H		Reserved		

Table 3.3 Allocation of internal parameter latch under write operation

Address Intel / Motorola		Name	Bit No.	Significance (Read Access!)
00H	01H	Int-Req-Reg	7..0	Interrupt Controller Register
01H	00H	Int-Req-Reg	15..8	
02H	03H	Int−Reg	7..0	
03H	02H	Int−Reg	15..8	
04H	05H	Status-Reg	7..0	Status Register
05H	04H	Status-Reg	15..8	
06H	07H	Mode-Reg 0	7..0	Setting parameters for individual bits
07H	06H	Mode-Reg 0	15..8	
08H		Mode-Reg1-S	7..0	
09H		Mode-Reg1-R	7..0	
0AH		WD_BAUD_CONTROL_Val	7..0	Root value for baud rate monitoring
0BH		MinTsdr_Val	7..0	minTSDR time
0CH		Reserved		
0DH				
0EH				
0FH				
10H				
11H				
12H				
13H				
14H				
15H				

3.3 Organization parameters

The cells in the address area 16H-3FH are mainly used to store organization parameters, such as device address, manufacturer ID, input/output buffer pointer and length. These units are read/write.

Address Intel / Motorola		Name	Bit No.	Significance (Read Access!)
16H		R_TS_Adr	7..0	Setup station address of the relevant APC3
17H		Reserved		Pointer to a RAM address which is presetted with 0FFH
18H	19H	R_User_Wd_Value	7..0	Based on an internal 16-bit wachdog timer, the user is monitored in the DP_Mode
19H	18H	R_User_Wd_Value	15..8	
1AH		R_Len_Dout_Puf		Length of the 3 Dout buffers
1BH		R_Dout_buf_Ptr1		Segment base address of Dout buffer 1
1CH		R_Dout_buf_Ptr2		Segment base address of Dout buffer 2
1DH		R_Dout_buf_Ptr3		Segment base address of Dout buffer 3
1EH		R_Len_Din_buf		Length of the 3 Din buffers
1FH		R_Din_buf_Ptr1		Segment base address of Din buffer 1
20H		R_Din_buf_Ptr2		Segment base address of Din buffer 2
21H		R_Din_buf_Ptr3		Segment base address of Din buffer 3
22H		Reserved		Preset with 00H.
23H				
24H		R Len Diag buf1		Length of Diag buffer 1
25H		R Len Diag buf2		Length of Diag buffer 2
26H		R_Diag_Puf_Ptr1		Segment base address of Diag buffer 1
27H		R_Diag_Puf_Ptr2		Segment base address of Diag buffer 2
28H		R Len Cntrl Pbuf1		Length of Aux buffer 1 and the control buffer belonging to it, for example, SSA-Buf, Prm-Buf, Cfg-Buf, Read-Cfg-Buf
29H		R Len Cntrl Pbuf2		Length of Aux-Buffer 2 and the control buffer belonging to it, for example, SSA-Buf, Prm-Buf, Cfg-Buf, Read-Cfg-Buf
2AH		R Aux Puf Sel		Bit array, in which the assignments of the Aux-buffers ½ are defined to the control buffers, SSA-Buf, Prm-Buf, Cfg-Buf
2BH		R_Aux_buf_Ptr1		Segment base address of auxiliary buffer 1
2CH		R_Aux_buf_Ptr2		Segment base address of auxiliary buffer 2
2DH		R_Len_SSA_Data		Length of the input data in the Set_Slave_Address-buffer
2EH		R SSA buf Ptr		Segment base address of the Set_Slave_Address-buffer
2FH		R_Len_Prm_Data		Length of the input data in the Set_Param-buffer
30H		R_Prm_buf_Ptr		Segment base address of the Set_Param-buffer
31H		R_Len_Cfg_Data		Length of the input data in the Check_Config-buffer
32H		R Cfg Buf Ptr		Segment base address of the Check_Config-buffer
33H		R_Len_Read_Cfg_Data		Length of the input data in the Get_Config-buffer
34H		R_Read_Cfg_buf_Ptr		Segment base address of the Get_Config-buffer
35H		Reserved		Preset with 00H.
36H				

37H		
38H		
39H	R_Real_No_Add_Change	This parameter specifies whether the DP slave address may again be changed at a later time point.
3AH	R_Ident_Low	The user sets the parameters for the Ident_Low value.
3BH	R_Ident_High	The user sets the parameters for the Ident_High value.
3CH	R_GC_Command	The Global_Control_Command last received
3DH	R_Len_Spec_Prm_buf	If parameters are set for the Spec_Prm_Buffer_Mode (see mode register 0), this cell defines the length of the param buffer.

Chapter 4. Register definition

The following describes the registers that affect APC3 hardware functions and protocol processing.

4.1 Mode register

The parameter bits that can be directly accessed or set by the controller are organized into two mode registers (0 and 1).

4.1.1 Mode register 0

The mode register 0 can be set only in the offline state (after power up). APC3 will exit the offline state only after all mode registers 0, all processor parameters and organization parameters (START_APC3=1, Mode Register1) are loaded.

Table 4.1 Mode register 0

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
06H (Intel)	Freeze_ Supported	Sync_ Supported	EARLY_ RDY	INT_ POL	MinTSDR				Mode Reg0 7..0

Address Control Register	Bit Position								Designation
	15	14	13	12	11	10	9	8	
07H (Intel)			Spec_Clear_Mode *)	Spec_Prm_Puf_Mode **)	WD Test		EOI Time base	DP Mode	Mode Reg0 15..8

*) When Spec_ Clear_ When Mode (Fail Safe Mode) =1, APC3 will receive a data message with a data length of 0 in the Data Exchange state. In the Data Exchange state, the response of the device to the output can be set in the parameterized message.

**) When a large number of parameters are transferred between the PROFIBUS master and slave, Aux Buffer 1/2 must be the same size as the parameterized buffer. Sometimes this may reach the limit of available storage space in APC3. When Spec_ Prm_ Puf_ When Mode=1, the data in the parameterized message can be directly processed in this specific buffer, so that the auxiliary buffer can be smaller.

Table 4.2 Mode register 0

Bit 0	
Bit 1	
Bit 2	
Bit 3	**minTSDR:** Default setting for the minTSDR after reset for DP operation or combi operation. 0 = Pure DP operation (default configuration!)
Bit 4	**INT_Pol:** Interrupt Polarity 0 = The interrupt output is low-active.
Bit 5	**Early_Rdy**: Early Ready 0 = Normal Ready: Ready is generated when data is valid (write) or when data has been accepted
Bit 6	**Sync_Supported:** Sync_Mode support 0 = Sync_Mode is not supported.
Bit 7	**Freeze_Supported**: Freeze_Mode support 0 = Freeze_Mode is not supported.
Bit 8	**DP_Mode:** DP_Mode enable 0 = DP_Mode is disabled.
Bit 9	**EOI_Time_Base:** End-of-Interrupt Timebase 0 = The interrupt inactive time is at least 1 us long.
Bit 10	
Bit 11	Test mode for the Watchdog-Timer, no function mode 0 = The WD runs in the function mode.
Bit 12	**Spec_Prm_Buf_Mode:** Special-Parameter-Buffer Mode 0 = No Special-Parameter-Buffer.
Bit 13	Special Clear Mode (Fail Safe Mode) 0 = No special clear mode.
Bit 15	

Note: The contents in the mode register 0 can only be modified in the offline state

4.1.2 Mode register 1

The mode register 1 contains some control bits that must be modified during operation. These control bits can be set separately (Mode_Reg_S) or reset separately (Mode_Reg_R). Use different addresses in the setting and reset operations, and write 1 to the corresponding position to indicate setting or reset.

Table 4.3 Mode register 1（Mode Register1 S/Mode Register1 R）

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
08H			Res_ User_WD	EN_ Change_ Cfg_Buffer	User_ Leave_ Master	Go_ Offline	EOI	START_ APC3	Mode-Reg_S 7..0
09H			Res_ User_WD	EN_ Change_ Cfg_Buffer	User_ Leave_ Master	Go_ Offline	EOI	START_ APC3	Mode-Reg_R 7..0

Bit 0	**Start_APC3:** Exiting the Offline state 1 = APC3 exits *offline* and goes to *passive-idle*. In addition, the idle timer and Wd timer are started
Bit 1	**EOI：** End of Interrupt
Bit 2	**Go_Offline：** Going into the offline state 1 = After the current requests ends, APC3 goes to the *offline state* and again sets Go_Offline to
Bit 3	**User_Leave_Master：** Request to the DP_SM to go to 'Wait_Prm.' 1 = The user causes the DP_SM to go to 'Wait_Prm.' After this action, APC3 sets User_Leave_Master
Bit 4	**En_Change_Cfg_Buffer：** Enabling buffer exchange (Cfg buffer for Read_Cfg buffer) 0 = With 'User_Cfg_Data_Okay_Cmd,' the Cfg buffer may not be exchanged for the Read_Cfg buffer.
Bit 5	**Res_User_Wd：** Resetting the User_WD_Timers 1 = APC3 again sets the User_Wd_Timer to the parameterized value 'User_Wd_Value15..0.' After

4.2 Status register

The status register maps the current status of APC3 and is read-only.

Table 4.4 Status register（RO）

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
04H	WD_State		DP_State		RAM access violation	Diag_ Flag		Offline/ Passive-Idle	Status-Reg 7...0
	1	0	1	0					

Address Control Register	Bit Position								Designation
	15	14	13	12	11	10	9	8	
05H					Baud Rate				Status-Reg 15...8
					3	2	1	0	

Bit 0	Offline/Passive-Idle：Offline-/Passive-Idle state 0 = APC3 is in offline.
Bit 1	
Bit 2	Diag_Flag：Status diagnostics buffer 0 = The DP master fetches the diagnostics buffer.
Bit 3	RAM Access Violation：Memory access > 1.5kByte 0 = No address violation 1 = For addresses > 1536 bytes, 1024 is subtracted from the current address, and there is access to this new
Bit 4,5	DP-State1..0：DP-State Machine state 00 = 'Wait_Prm' state 01= 'Wait_Cfg' state
Bit 6,7	WD-State1..0：Watchdog-State-Machine state 00 = 'Baud_Search' state 01= 'Baud_Control' state

	10 = 'DP_Control' state 11= Not possible
Bit 8,9,10,11	Baud rate3..0：The baud rates APC3 found 0000 = 12 MBaud 0001 = 6 MBaud 0010 = 3 MBaud 0011 = 1.5 MBaud 0100 = 500 kBaud 0101 = 187.5 kBaud 0110 = 93.75 kBaud 0111 = 45.45 kBaud 1000 = 19.2 kBaud 1001 = 9.6 kBaud Rest = Not possible
Bit	

4.3 Interrupt controller

The processor obtains information indicating messages and various error events through the interrupt controller. The interrupt controller can accommodate up to 16 events. These events are output through an interrupt, regardless of priority.

The interrupt controller includes interrupt request register (IRR), interrupt mask register (IMR), interrupt register (IR) and interrupt response register (IAR).

All events are stored in IRR, and each event can be prohibited through IMR. The input of IRR does not depend on the interrupt mask.

The unmasked events in MR will generate X/INT interrupt.

Note: Users can write IRR to manually set each event for debugging.

Each interrupt event processed by the processor must be deleted (i.e. confirmed) through IAR (except New_Prm_Data, New_DDB_Prm_Data and New_Cfg_Data), which is implemented at the corresponding bit position 1. If a new event and the confirmation of the previous event appear in the IRR at the same time, the event will be saved. If the processor subsequently enables a mask, it must ensure that no input events exist in the IRR. For security purposes, you must delete the corresponding bit in the IRR before setting the IMR.

Before exiting the interrupt program, the processor must set "end of interrupt signal (E01)=1" in the mode register. The interrupt signal is cancelled by changing the signal edge. If another event also needs to be stored, the interrupt output will wait for at least 1 usec or 1-2ms of interrupt inactivity before being activated. This interrupt inactivity time can be set through "EOI_Timebase". This makes it possible to enter the interrupt program when the interrupt is triggered using the signal edge.

The polarity of interrupt output passes INT_ Pol mode bit. After the hardware reset, the interrupt output is low.

Table 4.5 Interrupt request register (RW)

Address	Bit Position								Designation
Control	7	6	5	4	3	2	1	0	
00H					WD_DP _Mode_	Baud_ rate_	Go/Leave Data_EX	MAC_ Reset	Int-Req-Reg 7..0

Address	Bit Position								Designation
Control	15	14	13	12	11	10	9	8	
01H			DX_O UT	Diag_ Buffer_ Changed	New_Pr m_Data	New_Cf g_Data	New_SSA _Data	New_GC Command	Int-Req-Reg 15 .. 8

Bit 0	MAC_Reset After it processes the current request, the APC3 has arrived at the offline state (through setting the 'Go_Offline bit' or through a RAM access violation).
Bit 1	Go/Leave_DATA_EX The DP_SM has entered or exited the 'DATA_EX' state.

Bit 2	Baudrate_Detect The APC3 has exited the 'Baud_Search state' and found a baud rate.
Bit 3	WD_DP_Control_Timeout The watchdog timer has run out in the 'DP_Control' WD state.
Bit 4	
Bit 5	Res For additional functions
Bit 6	Res For additional functions
Bit 7	Res For additional functions
Bit 8	New_GC_Command The APC3 has received a 'Global_Control telegram' with a changed 'GC_Command-Byte,' and this byte is stored in the 'R_GC_Command' RAM cell.
Bit 9	New_SSA_Data The APC3 has received a 'Set_Slave_Address telegram' and made the data available in the SSA buffer.
Bit 10	New_Cfg_Data The APC3 has received a 'Check_Cfg telegram' and made the data available in the Cfg buffer.
Bit 11	New_Prm_Data The APC3 has received a 'Set_Param telegram' and made the data available in the Prm buffer.
Bit 12	Diag_Buffer_Changed Due to the request made by 'New_Diag_Cmd,' APC3 exchanged the diagnostics buffer and again made the old buffer available to the user.
Bit 13	DX_OUT The APC3 has received a 'Write_Read_Data telegram' and made the new output data available in the N buffer. For a 'Power_On' or for a 'Leave_Master,' the APC3 deletes the N buffer and also generates this interrupt.
Bit 14	Res For additional functions
Bit 15	Res For additional functions

Refer to IRR for allocation of bits of other interrupt control registers.

Table 4.6 Other interrupt control registers

Address	Register		Reset State	Assignment	
02H/03H	Interrupt Register	Readable	All bits deleted		
04H/05H	Interrupt Mask Register (IMR)	Writable, can be changed during operation	All bits set	Bit = 1 Bit = 0	Mask is set and the interrupt is disabled. Mask is deleted and the interrupt is enabled.
02H/03H	Interrupt Acknowledge Register	Writable, can be changed during operation	All bits deleted	Bit = 1 Bit = 0	The IRR bit is deleted. The IRR bit remains unchanged.

New_Prm_Data" "New_Cfg_Data" events cannot be deleted by interrupting the acknowledge register. Instead, users need to delete events through "Confirm Operation" (for example, "User_Prm_Data_Okey") o

4.4 Watchdog Clock

4.4.1 Automatic baud rate recognition

APC3 can automatically identify the baud rate. After each reset, or after the watchdog timer times out, APC3 will enter the "baud rate search" state.

In the process of automatic baud rate recognition, APC3 searches from the highest baud rate. If no complete and error free SD1 and SD2 message is received within a given monitoring time, the baud rate search will continue at the next lower baud rate.

After identifying the correct baud rate, APC3 switches to the "Baud_Control" state and monitors the baud rate. The monitoring time can be set by the user with parameter WD_ Baud_ Control_ Val. The watchdog operates at a frequency of 100Hz (10msec). The watchdog will reset after receiving each message sent to the device address without error. If the timer times out, APC3 will switch to the baud search state again.

4.4.2 Baud rate monitoring

APC3 will continuously monitor the determined baud rate in the "Baud_Control" state. After receiving each message sent to the corresponding address of the device without error, the watchdog timer will be reset. The monitoring time value is set by the user as parameter WD_ Baud_ Control_ Val is obtained by multiplying by the time base (10ms). If the watchdog timer times out, WD_ SM will enter the "Baud_Search" state again. If the user sets APC3 to execute DP protocol mode (DP_Mode=1, see mode register 0), after receiving the "Set_Param telegram" message from the master station and WD_ When On=1, the watchdog will be used to monitor the "DP_Control" status. When receiving "Set_Param telegram" message and WD_ When On=0, the watchdog keeps monitoring the baud rate. When the timer is timed out, the PROFIBUS DP state machine is still not reset. For example, the slave station is still in the "DATA_Exchange" state.

4.4.3 Response time monitoring

The "DP_Control" status serves the response time monitoring of the DP master (Master_Add). The monitoring time value is obtained by multiplying the product of two watchdog factors and the current effective time base (1ms or 10ms).

TWD=(1ms or 10ms) * WD_ Fact_ 1 * WD_ Fact_ 2 (See 7 bytes in parameterized message). It should be noted that WD_ Fact_ 1 and WD_ Fact_ 2 The user cannot modify it. It is set by the master station; The current valid time base is set in the mode register 0.

The monitoring time range is between 1ms and 650s, independent of baud rate.

If the monitoring timer times out, APC3 will enter the "Baud_Control" state again, and APC3 will generate the "WD_DP_Control_Timeout Interrupt" event. In addition, the DP status is reset.

If another master station accepts APC3, when WD_ When On=0, APC3 will enter the "Baud_Control" state; When WD_ When On=1, APC3 will enter the "DP_Control" state.

Chapter 5. PROFIBUS-DP Interface

5.1 DP Buffer Structure

DP mode is enabled with DP_Mode=1 (see mode register 0). In this process, the following SAPs are fixed for DP mode.

- Default SAP: Data exchange (Write_Read_Data)
- SAP53: reserved
- SAP55: Changing the station address (Set_Slave_Address)
- SAP56: Reading the inputs (Read_Inputs)
- SAP57: Reading the outputs (Read_Outputs)
- SAP58: Control commands to the DP-Slave (Global_Control)
- SAP59: Reading configuration data (Get_Config)
- SAP60: Reading diagnostics information (Slave_Diagnosis)
- SAP61: Sending parameter setting data (Set_Param)
- SAP62: Checking configuration data (Check_Config)

The APC3 integrates the DPV0 part of the DP slave protocol. The user must configure the ASIC accordingly and process and acknowledge the received information. The SAPs are always enabled, except for default SAP, SAP56 and SAP58. The default SAP, SAP56 and SAP58 are only enabled when the DP slave state machine (DP_SM) enters the "DATA_EX" state. The user has the right to disable SAP55, i.e. to disable the master from modifying the slave address, when the corresponding buffer pointer R_SSA_Puf_Ptr must be set to 00H. The DDB function is disabled through the initialization process of the RAM cell.

Figure 5.1 shows the DP_SAP buffer structure. The user needs to configure all buffers in the "offline state" (length and buffer start address, indicated by segment number). During the operation of APC3, the buffer configuration is not allowed to change except for the length of the Dout-Din buffer.

After receiving the configuration message (Check_Config), the user can modify the Dout-Din buffer configuration in the "Wait_Cfg" state. In the "DATA_EX" state, only the same configuration can be accepted.

The buffer structure is divided into: data buffer, diagnostic buffer and control buffer.

The output data and input data each have three available buffers of the same length. These buffers function like swap buffers. One buffer is assigned to the "D" data transfer and the other buffer is assigned to the "U" user. The third buffer is in the Next "N" state or the Free "F" state.

Two variable length diagnostic buffers are used to store diagnostic data. One of the diagnostic buffers is always in the "D" state for APC3 to send diagnostic data. The other diagnostic buffer is assigned to the user and is in the "U" state and is used to prepare new diagnostic data.

APC3 first reads the different parameter setting messages (Set_Slave_Address, Set_Param) and configuration messages (Check_Config) and saves them to Aux-Buffer1 or Aux-Buffer2....

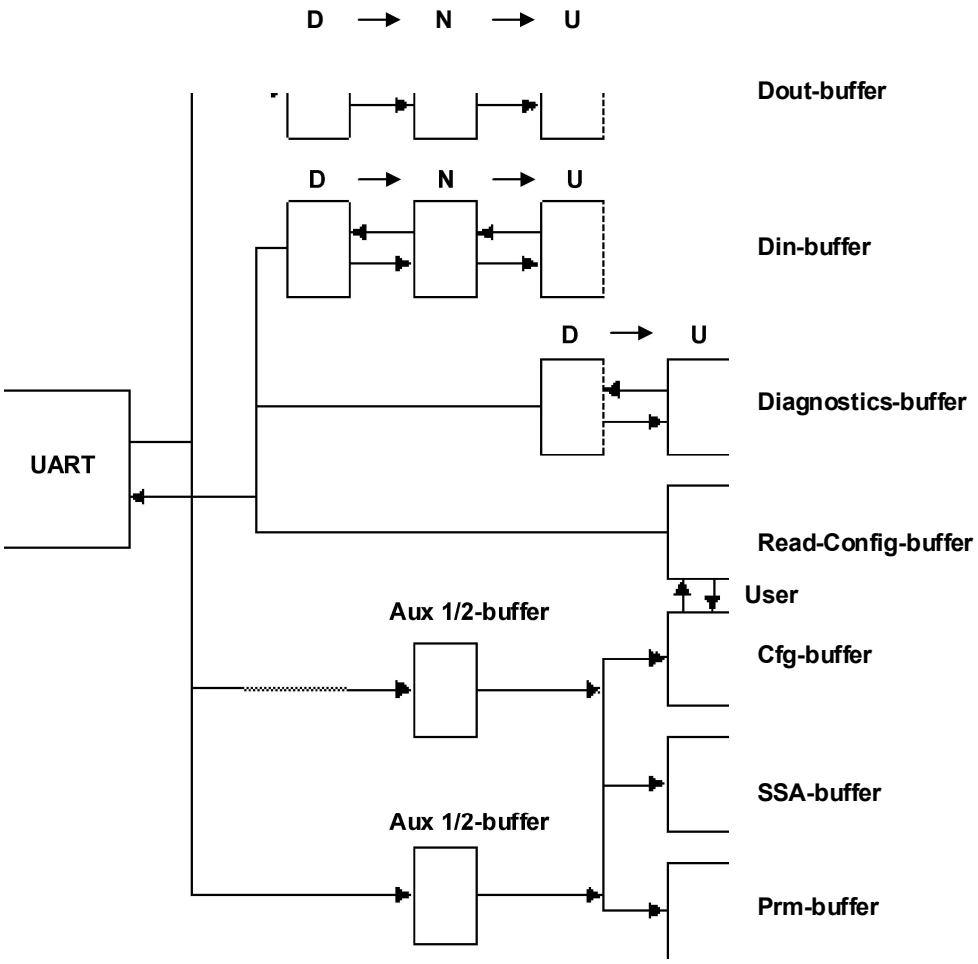

Figure 5.1 DP_SAP buffer structure

The data exchange takes place by means of in the corresponding target buffers (SSA-buffer, Prm-buffer, Cfg-buffer). Each set of buffers must have the same length. In the "R_Aux_Puf_Sel" parameter cell, the user defines which Aux_buffers are used to buffer that kind of messages. If the data definition of these DP messages is different, as in the case of the Set_Prm message, which has a significantly larger amount of data than the other messages, it is better to use Aux_Buffer2 (Aux_Sel_Set_Param=1). Other messages are read by Aux_Buffer1 (Aux_Sel...=0). If the buffer is too small, APC3 will respond with "no resources".

Table 5.1 Aux_Buffer management

Address RAM Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
2AH						Set_Slave_Adr	Check_Cfg	Set_Prm	R_Aux_Puf_Sel
						X1	X1	X1	See below for coding.

X1	Coding
0	Aux_Buffer1
1	Aux_Buffer2

In the Read-Cfg-buffer, the user provides the configuration data (Get_Config) for the master to read. the length of the Read-Cfg-buffer must be the same as the Cfg-buffer.

Read_Input_Data insulation operates in the Din-buffer in the "D" state, and Read_Output_Data insulation operates in the Dout-buffer in the "U" state.

All buffer pointers are 8-bit segment addresses because APC3 has only 8-bit address registers internally. When accessing RAM, APC3 shifts the segment address left by 3 bits plus the 8-bit intra-segment offset address to obtain an 11-bit address.

APC3 adds an 8-bit offset address to the 3-bit conversion of the segment address (result: 11-bit physical address).

5.2 DP Service Description

5.2.1 Set_Slave_Address（SAP55）

In general, the address of the slave can be set in the following way:

- Modifying the slave's address with a service message via a Class II master, which is commonly used by PA meters to set addresses;
- A dipswitch is installed in the slave to set the address, and most DP slaves use this method.

A slave can have its address modified by a Class II master only when the device is in the Wait_Prm state.

The user can disable the device slave address function by setting R_SSA_Puf_Ptr=00H. In this case, user can set the slave address by dipswitch and then write the address to R_TS_Adr RAM register.

The user must provide a non-volatile memory (e.g., EEPROM) to support this function. The external EEPROM must be able to store the new "station address" and the "Real_No_Add_Change" parameter ("True"=FFH). When Real_No_Add_Change=True, the slave address can be changed only once.

The R_TS_Adr and R_Real_No_Add_Change parameters saved in the EEPROM are provided to APC3 by the user after each power-up boot.

If SAP55 is activated and the Set_Slave_Address message is received correctly, APC3 saves the service data in the Set_Slave_Address message to Aux_Puffer1/2 and copies the data in Aux_Buffer1/2 to SSA_Buffer, storing the data length in R_ Len_SSA_Data, and then generate New_SSA_Data interrupt. The user needs to save the new "Station Address" and the new "Real_No_Add_Change" parameters. The user does not need to write these changed parameters back to APC3.

After reading these buffers, the user performs the SSA_Buffer_Free_Cmd operation (read 14H address) to complete the acknowledgement. This acknowledgement operation will make APC3 ready to receive the next set slave address message again (e.g. from another master).

APC3 takes care of any errors that may occur in it on its own.

Table 5.2 SSA_Buffer_Free_Cmd Coding

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
14H	0	0	0	0	0	0	0	0	SSA_Puffer_Free_Cmd
	Don’t care								

5.2.2 Set_Param (SAP61）

The Class II master assigns to the slave the parameters required for communication with the slave via the Set_Param service, and specifies the operating status. At the same time, the slave is informed of the address of the master with which it is communicating.

The data in the Set_Param service consists of standard parameters and user parameters, where the user parameters are determined by the instrumentation device manufacturer, and these user parameters are described in the GSD file.

APC3 first analyzes the first seven bytes (standard parameter part, excluding user prm data), or the first eight bytes (standard parameter part, plus DPV1_Status_1). The meaning of the first seven bytes is specified by the standard. The eighth data byte is used to specify APC3 features, such as support or not for DPV1. The rest of the data belongs to the user application section.

Upon receipt of a properly parameterized message, APC3 performs the following actions:

APC3 swaps the data in Aux_Buffer1/2 into Prm-buffer, saves the data length in R_Len_Prm_Data, and triggers the New_Prm_Data interrupt. The user must check the User_Prm_Data data and confirm the result by User_Prm_Data_Okay_Cmd or User_Prm_Data_Not_Okay_Cmd. The buffer contains the entire message, i.e., the application-related parameters start only from the 8th byte.

Note: The user response (User_Prm_Data_Okay_Cmd or User_Prm_Data_Not_Okay_Cmd) will trigger the New_Prm_Data interrupt again. The user does not have to acknowledge the New_Prm_Data interrupt in the IAR register.

When the user gives the User_Prm_Data_Not_Okay_Cmd confirmation result, APC3 sets the relevant diagnostic bit in the diagnostic message and enters the "Wait_Prm" state.

Read access to the corresponding registers means that User_Prm_Data_Okay_Cmd and User_Prm_Data _Not_Okay_Cmd responses can be acknowledged.

- “User_Prm_Finished”： No additional parameterized messages exist
- “Prm_Conflict”： There is an additional parameter message present, processed again
- “Not_Allowed”： Access is not allowed in the current bus state

Table 5.3 User_Prm_Data_Not/_Okay_Cmd Coding

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
0EH	0	0	0	0	0	0	↓	↓	User_Prm_Data_Okay
							0	0	User_Prm_Finished
							0	1	Prm_Conflict
							1	1	Not_Allowed

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
0FH	0	0	0	0	0	0	↓	↓	User_Prm_Data_Not_Okay
							0	0	User_Prm_Finished
							0	1	Prm_Conflict
							1	1	Not_Allowed

If there is another Set_Param message to be received at the same time, Prm_Conflict is returned in the previous Set_Param message acknowledgement, either positive or negative. The user has to repeat this process, because APC3 has provided a new Prm-buffer.

5.2.3 Check_Config（SAP62）

After successful parameterization, the master starts sending Check_Config messages to each slave, defining the structure of the Input/Output data to be exchanged.

Note: The slaves mentioned here do not refer to online slaves, but to slaves involved in system control applications, excluding slaves that are only powered on but not involved in system control applications.

The user processor needs to check and evaluate the configuration data. When APC3 receives a valid Check_Config message, APC3 will swap the data in Aux_Puffer1/2 to Cfg-buffer, save the data length in R_Len_Cfg_Data, and generate New_Cfg_Data interrupt.

After checking User_Config_Data, the user needs to confirm the check result with User_Cfg_Data_Okay _Cmd or User_Cfg_Data_Not_Okay_Cmd. The configuration data is saved in the Cfg-buffer in the standard d efined format.

User acknowledgement via "User_Cfg_Data_Okay_Cmd" or "User_Cfg_Data_Not_Okay_Cmd" will ge nerate the "New_Cfg_Data interrupt again and will not be acknowledged in the IAR register.

If the configuration check is incorrect, APC3 will modify the corresponding diagnostic bits in the diagnostic information and will enter the "Wait_Prm" state. If the configuration is correct, the APC3 will immediately enter the "DATA_EX" state if no Din_Buffer exists (R_Len_Din_Puf=00H) and set the counters for parameterization and configuration messages to 0. Otherwise, only the user can write the input data in the free otherwise, APC3 will enter the "DATA_EX" state only when the user writes input data in the free "N" buffer and executes the "New_Din_Puffer_Cmd" command. state and the "Go/Leave_Data_Exchange" interrupt is generated.

If the message data received from the Cfg buffer causes the "Read_Cfg" buffer to change (i.e., the configuration data changes), before the "User_Cfg_Data_Okay_Cmd" acknowledgement can be made, the user The new Read_Cfg data must be validated. If "EN_Change_Cfg_Buffer=1" is set in mode register 1 after receiving the confirmation, APC3 will update the Cfg buffer with the contents of the Read_Cfg buffer.

During the acknowledgement process, the user receives a message about whether there is a conflict. If another Check_Config message is received at the same time, the user will get a "Cfg_Conflict" message when acknowledging the previous Check_Config message, either positive or negative. The user must then repeat

this process, as APC3 has provided a new Cfg-buffer.

The "User_Cfg_Data_Okay_Cmd" and "User_Cfg_Data_Not_Okay_Cmd" confirmation operations are performed by reading the corresponding register cells and then obtaining the "Not_Allowed", "User_Cfg_Finished" or "Cfg_Conflict" information.

Table 5.4 User_Cfg_Data_Not/_Okay_Cmd Coding

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
10H	0	0	0	0	0	0	↓	↓	User_Cfg_Data_Okay
							0	0	User_Cfg_Finished
							0	1	Cfg_Conflict
							1	1	Not_Allowed

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
11H	0	0	0	0	0	0	↓	↓	User_Cfg_Data_Not_Okay
							0	0	User_Cfg_Finished
							0	1	Cfg_Conflict
							1	1	Not_Allowed

5.2.4 Slave_Diagnosis (SAP60)

The master uses the Slave_Diagnosis service to obtain the operating status of the slave to determine the next step in the operation process. The diagnostic response data returned by the slave includes 6 bytes of standard data, and user-specific diagnostic data (optional).

After the system enters the "DATA_EXCH" state, if the slave station has a fault and needs to send an alarm, the slave station will send a data exchange response message in the form of a high-priority message indicating that the slave station has diagnostic information (including alarm information) to send, and the master station will send a diagnostic request to take the diagnostic information in the next work cycle.

5.2.4.1 Processing Flow

APC3 provides two buffers for diagnostic processing. The length of these two buffers can be changed. One buffer is used for APC3 to send diagnostic data, and the user can process new diagnostic data in parallel in the other buffer. If new diagnostic data needs to be sent, then the user needs to exchange the two diagnostic buffers with the "New_Diag_Cmd" operation. The user gets the confirmation of successful buffer exchange through Diag_Puffer_Changed interrupt.

The internal "Diag_Flag" flag is set when the buffer is swapped. For the activated "Diag_Flag" flag, APC3

will send the next Write_Read_Data with high priority to inform the corresponding master that there is diagnostic data to be sent in the slave. If the user sets Diag.Stat_Diag=1, then Diag.Stat_Diag will remain active until the corresponding master has picked up the diagnostic data. The user can poll the Diag_Flag flag bit in the status register to know whether the master has picked up the new diagnostic data.

Description: When the processor finds that the device has "Ext_Diag", "Stat_Diag" and "Ext. Diag_Overflow", it is necessary to set the lower three digits in the first byte of the diagnostic information respectively.

Table 5.5 Diag_Buffer Allocation

Address RAM Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
0CH	0	0	0	0	D_Puf2		D_Puf1		Diag_Puffer_SM
					X1	X2	X1	X2	See below for coding.

X1	X2	Coding
0	0	Each for the D_Buf2 or D_Buf1
0	1	User
1	0	APC3
1	1	APC3_Send_Mode

The New_Diag_Cmd command is a read operation on the selected storage unit to know which buffer will be allocated to the user after the diagnostic buffer swap or if both buffers are allocated to APC3 ("no Puffer", "Diag_Puf1 ", "Diag_Puf2").

Table 5.6 Diag_Puffer_SM， New_Diag_Cmd codes

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
0DH	0	0	0	0	0	0	↓	↓	New_Diag_Cmd
							0	0	no Puffer
							0	1	Diag_Puf1
							1	0	Diag_Puf2

5.2.4.2 Diagnostic Buffer Structure

The user organizes the diagnostic data in the format given in the figure below. The first 6 bytes are placeholders, except for the lower three of the first byte, i.e. they do not require user intervention. The user saves the contents of the lower three first bytes, i.e. "Diag. ". When transmitting, APC3 will preprocess the first 6 bytes according to the standard.

Table 5.7 Diagnostic Buffer Structure

Byte	Bit Position								Designation
	7	6	5	4	3	2	1	0	

0						Ext.Diag_Overflow	Stat_Diag	Ext_Diag	
1									
2									
3									
4									
5									
6									
6~n	user input								Ext_Diag_Data (n = max. 243)

The user's external diagnostic data (Ext-Diag_Data) follows the first 6 bytes and is loaded into the diagnostic buffer. There are three different modes of external diagnostic data (device related, ID related and channel related). In addition to "Ext_Diag_Data", the buffer length also contains the standard diagnostic data (6 bytes) (R_Len_Diag_Puf1, R_Len_Diag_Puf2).

5.2.5 Write_Read_Data / Data_Exchange (Default_SAP)

5.2.5.1 Writing Outputs

The Class II master writes output data directly to the slave through the Writing Outputs service without the DATA_EXCHANGE service. It is mainly used for debugging of devices and systems.

APC3 reads the received output data from the "D" buffer. After receiving without errors, APC3 will convert the new buffer from "D" to "N" and generate a DX_Out_Interrupt. The user gets the new output data from "N". The buffer is transformed from "N" to "U" by "Next_Dout_Buffer_Cmd" command, so the master can get the output data from the slave through Read_Out_Interrupt service. Outputs service to get the output data from the slave.

When the user's processing time is less than the bus cycle time, the user will receive the same data several times. In the case of 12Mbd baud rate, it is likely that the user's processing time will be larger than the bus cycle time, and then the user will lose some data and receive only the latest data.

Under "Power_On", "Leave_Master" and "Global_Control_Telegram_Clear" APC3 will delete the D-buffer and then switch it to "N". This also happens at power-up (when it goes to the "Wait_Prm" state). If the user reads this buffer at this time, he will receive a "U_buffer cleared" indication when performing the "Next_Dout_Buffer_Cmd" operation. If the user needs to increase the output data buffer after receiving the Check_Config message, the user must delete the data in the N-buffer himself (only happens in the "Wait_Cfg" state after power-up).

If "Diag.Syne_Mode=1", the D-buffer will be filled and no swapping will occur when a Write_Read_Data-Telegram message is received, but it will be swapped according to the synchronous or asynchronous command in the next Global_control message. The user can read the buffer operation status by the following four status codes: "Nil", "Dout_Puf_Ptrl-3". The pointer to the current data is in the "N" state.

Table 5.8 Dout_Buffer Management

Address	Bit Position	Designation

Control Register	7	6	5	4	3	2	1	0	
0AH	F		U		N		D		Dout_Puffer_SM
	X1	X2	X1	X2	X1	X2	X1	X2	See below for coding.

X1	X2	Coding
0	0	Nil
0	1	Dout_Puf_ptr1
1	0	Dout_Puf_ptr2
1	1	Dout_Puf_ptr3

When reading "Next_Dout_Buffer_Cmd", the user is informed which buffer (U-buffer) belongs to the user after the buffer swap, or if the replacement has occurred.

Table 5.9 Next_Dout_Puffer_Cmd

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
0BH	0	0	0	0	U_Buffer	State_U_Buffer	Ind_U_Buffer		Next_Dout_Buf_Cmd
							0	1	Dout_Puf_ptr1
							1	0	Dout_Puf_ptr2
							1	1	Dout_Puf_ptr3
						0			No new U buffer
						1			New U buffer
					0				U buffer contains data
					1				U buffer are deleted

The user must delete the U-buffer at initialization, allowing the defined (or deleted) data to be sent to the master via Read_Output messages before the first data cycle.

5.2.5.2 Reading Inputs

Class II masters read the input data in the slave directly through the Reading Inputs service without going through the DATA_EXCHANGE service. It is mainly used for debugging of devices and systems.

APC3 sends the input data from the D buffer. Before sending, APC3 will swap "N" and "D". If there is no new input data, no buffer swap will occur.

The user prepares new input data in "U", and the buffer will be updated from "U" to "N" by "New_Din_buffer_Cmd" command. "N". If the user prepares the data in less time than the bus cycle time, not all new input data will be sent, but the latest data will be sent. However, at 12Mbd baud rate, it is more likely that the cycle time for user ready data is greater than the bus cycle time, and the APC3 will send the same data several times in a row.

During startup, after all parameter messages and configuration messages are acknowledged, APC3 first

enters the "DATA_EX" state before the user can use the "New_Din_Buffer_Cmd" operation to get the first valid Din buffer in "N" to get the first valid Din buffer.

If "Diag.Freeze_Mode=1", there will be no buffer swapping before sending. The user can get the state of the state machine by coding the following four states: "Nil", "Dout_Puf_Ptr1-3" the pointer to the current data is in the "N " state.

Table 5.10 Din_Buffer Management

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
08H	F		U		N		D		Din_Puffer_SM
	X1	X2	X1	X2	X1	X2	X1	X2	See below for coding.

X1	X2	Coding
0	0	Nil
0	1	Din_Puf_ptr1
1	0	Din_Puf_ptr2
1	1	Din_Puf_ptr3

When reading "New_Din_Buffer_Cmd", the user will get the information which buffer (U-buffer) belongs to the user after the buffer swap, i.e. Din_Buf_Ptr1-3.

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
09H	0	0	0	0	0	0	↓	↓	New_Din_Buf_Cmd
							0	1	Din_Puf_ptr1
							1	0	Din_Puf_ptr2
							1	1	Din_Puf_ptr3

5.2.5.3 User Watchdog Timer

After the device is powered up and enters the "DATA_EX" state, it is possible that the user continuously receives Write_Read_Data-telegrams, but the user does not operate the input/output buffers. If the user processor "hangs", the master will not know about it. Therefore, a "user watchdog timer" is needed to monitor the status of the user processor.

User_Wd_Timer is an internal 16-bit RAM unit that starts from the user-set "R_User_Wd_Value15.0" value and decrements with each Write_Read_Data message received in the APC3. If the timer value decreases to 0, APC3 will transition to the "Wait_Prm" state and DP_SM will enter the "Leave_Master" state. The user must set this cyclically

The initial value of the timer, i.e. Res_User_Wd=1, is constantly set in the mode register 1. Each time a Write_Read_Data message is received, APC3 loads "R_User_Wd_Value15.0" into User_Wd_Timer again and sets "Res_User_Wd=0" (mode register 1). and set "Res_User_Wd=0" (mode register 1). During power-up, the

user must set "Res_User_Wd=1".

5.2.6 Global_Control（SAP58）

APC3 processes Global_Control messages independently. Moreover, the user can also access the information in the Global_Control message. The first byte of data for a valid Global_Control command is stored in the R_GC_Command RAM cell, and the second byte of data (Group_Select) is processed internally by the chip without user intervention.

Table 5.11 Data format of the Global_Control message

Address	Bit Position								Designation
Control	7	6	5	4	3	2	1	0	
3CH	Res	Res	Sync	Unsync	Freeze	Unfreeze	Clear_Data	Res	R_GC_Command

Bit	Designation	Significance
0	Reserved	
1	Clear_Data	With this command, the output data is deleted in ‘D’ and is changed to ‘N.’
2	Unfreeze	With „Unfreeze,“ freezing input data is cancelled.
3	Freeze	The input data is fetched from ‘N’ to ‘D’ and „frozen“. New input data is not fetched again until the master sends the next ‘Freeze’ command.
4	Unsync	The „Unsync“ command cancels the „Sync“ command.
5	Sync	The output data transferred with a WRITE_READ_DATA telegram is changed from ‘D’ to ‘N.’ The following transferred output data is kept in ‘D’ until the next ‘Sync’ command is given.
6,7	Reserved	The „Reserved“ designation specifies that these bits are reserved for future function expansions.

If the Control_Comand bit is changed in the latest received Global_Control message, APC3 generates a "New_GC_Command" interrupt. During the initialization process, APC3 pre-sets the "R_GC_Command" unit to 00H.

The user can read and analyze this unit.

To support Sync and Freeze functions, enable in mode register 0 is required.

5.2.7 Read_Inputs（SAP56）

APC3 uses the Read_Inputs message to get the input data just like the Write_Read_Data message. Before sending, if new input data is available in "N", "N" will be converted to "D". For "Diag.Freeze_Mode=1", no buffer conversion will occur.

5.2.8 Read_Outputs（SAP57）

APC3 gets the output data from the Dout buffer in the "U" state. At power-up, the user must pre-set the output data to "0" so that no invalid data is sent here. If there is a buffer change from "N" to "U" between the first call and the repeat (via Next_Dout_Buffer_Cmd), the new output data is sent during the repeat.

5.2.9 Get_Config（SAP59）

The user provides configuration data in the Read_Cfg buffer. For configuration changes generated after the Check_Config message, the user writes this change data in the Cfg buffer, sets "EN_Change_Cfg_buffer=1" (see mode register 1), and then APC3 exchanges the Cfg buffer and Read_Cfg buffer. If one of the configuration data changes during operation (e.g. for modular DP systems), the user must return APC3 to the "Wait_Prm" state with "Go Offline".

Chapter 6. Hardware design

This chapter gives the hardware connection principle under different processor interface modes.

6.1 Interface Configuration

APC3 configures the processor interface through two pins (XINT/MOT, MODE or). See Figure 6.1 or processor selection.

Table 6.1 Processor interface

XINT/MOT	MODE	Processor Interface Mode
0	1	Synchronous Intel mode
0	0	Asynchronous Intel mode
1	0	Asynchronous Motorola mode
1	1	Synchronous Motorola mode

6.2 Application Examples (Principles)

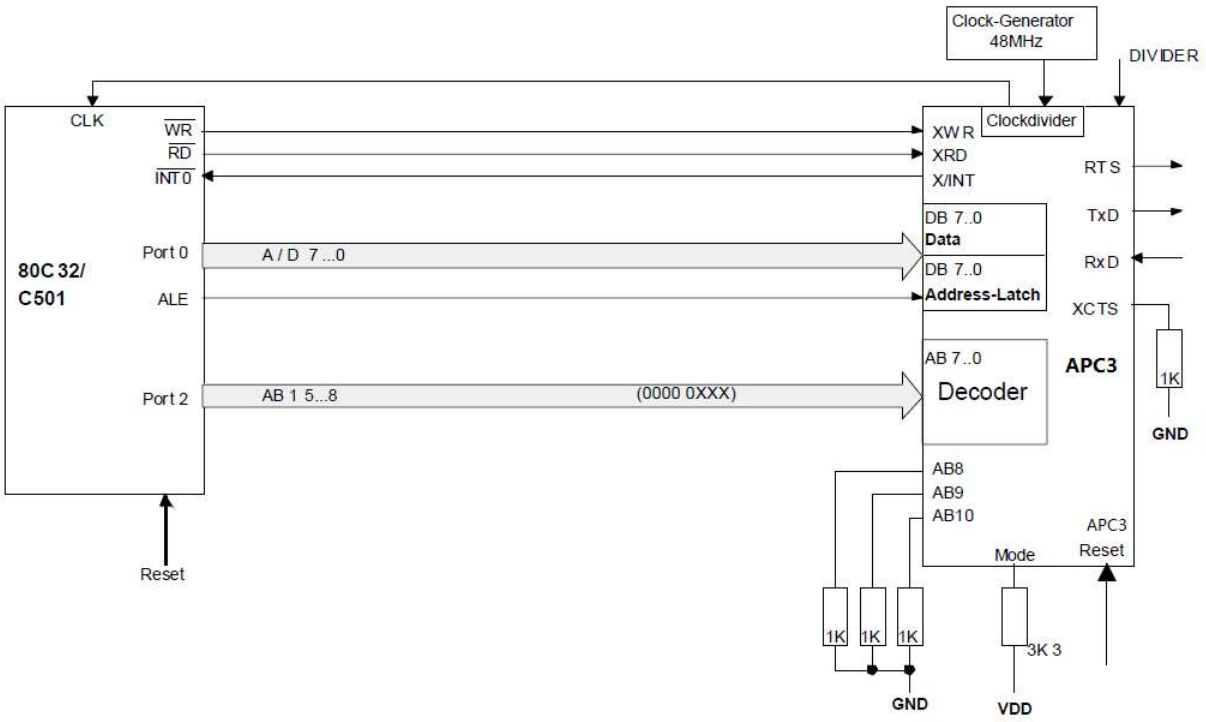

Figure 6.1 Low Cost System with 80C32

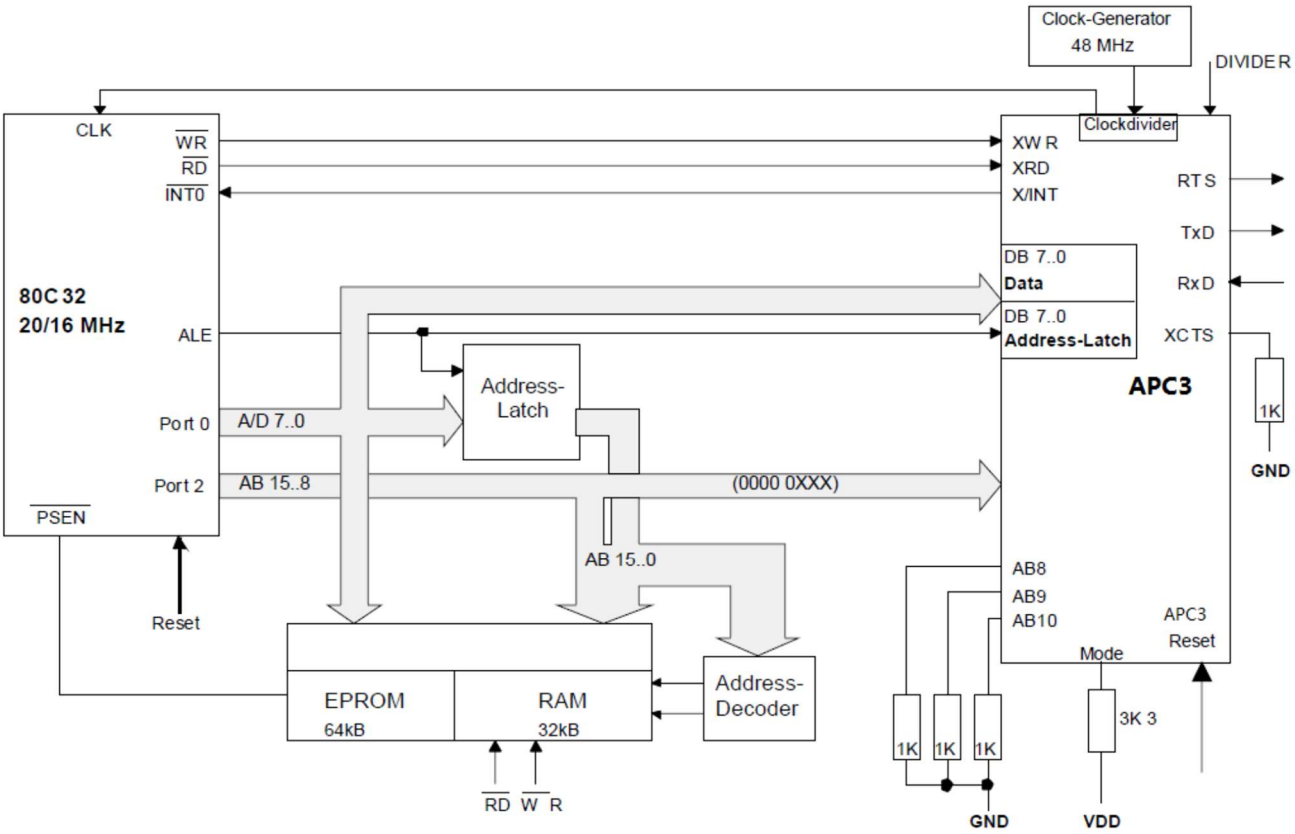

Figure 6.280C32 System with External Memory

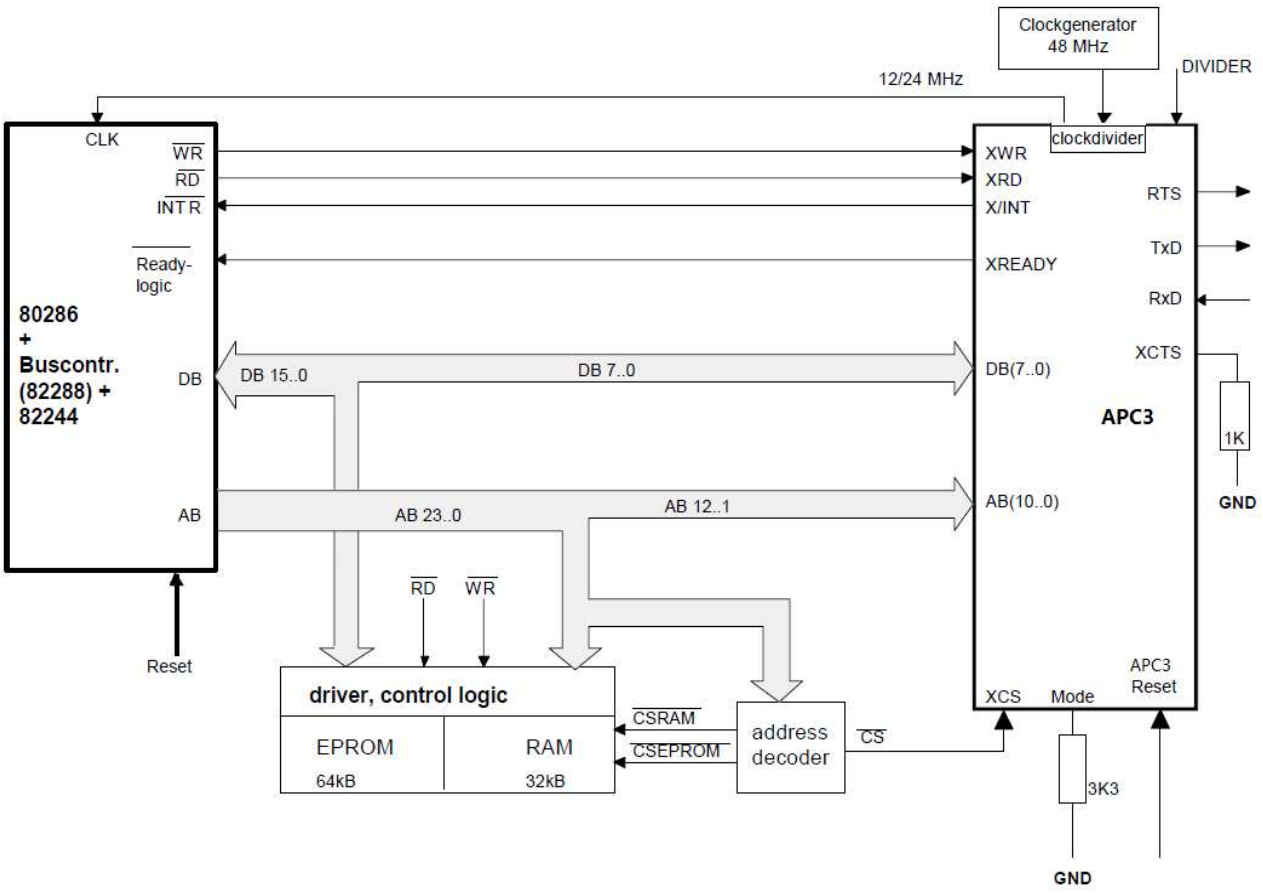

Figure 6.3 80286 System (X86 Mode)

6.3 Application with the 80C32

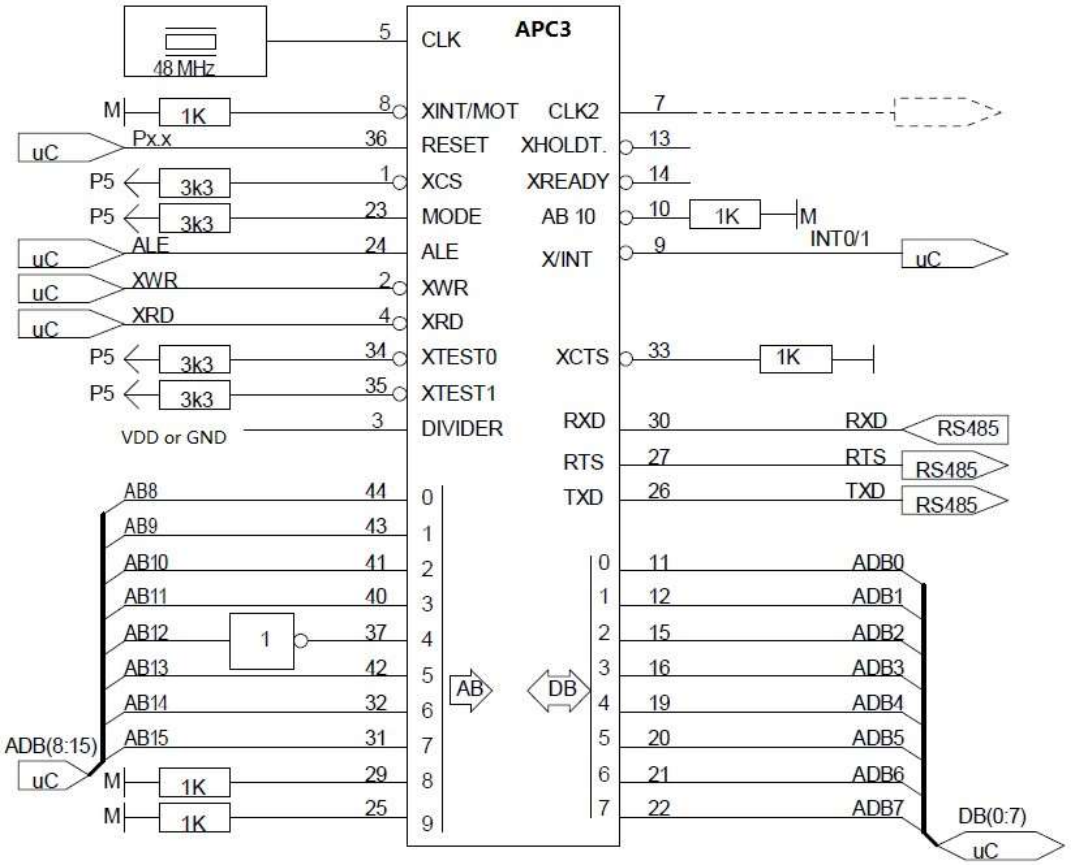

Figure 6.4 80C32 Application

The pull-up/pull-down resistor in the above figure is only available on the circuit tester. When address lines A11... A15 are set to 0, internal chip logical units are available. In the above example, the starting address of APC3 is set to 0X1000.

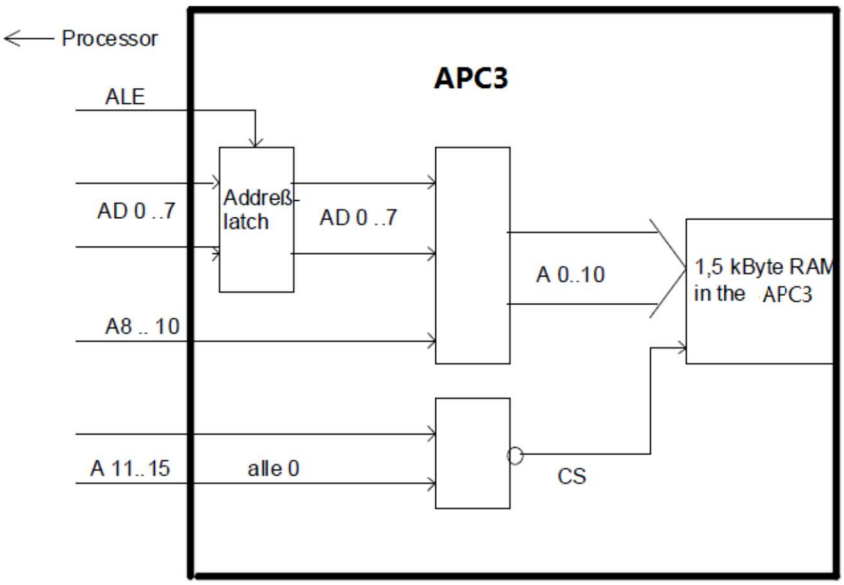

Figure 6.5 Internal Chipselect Generation in Synchronous Intel Mode

6.4 Application with the 80C165

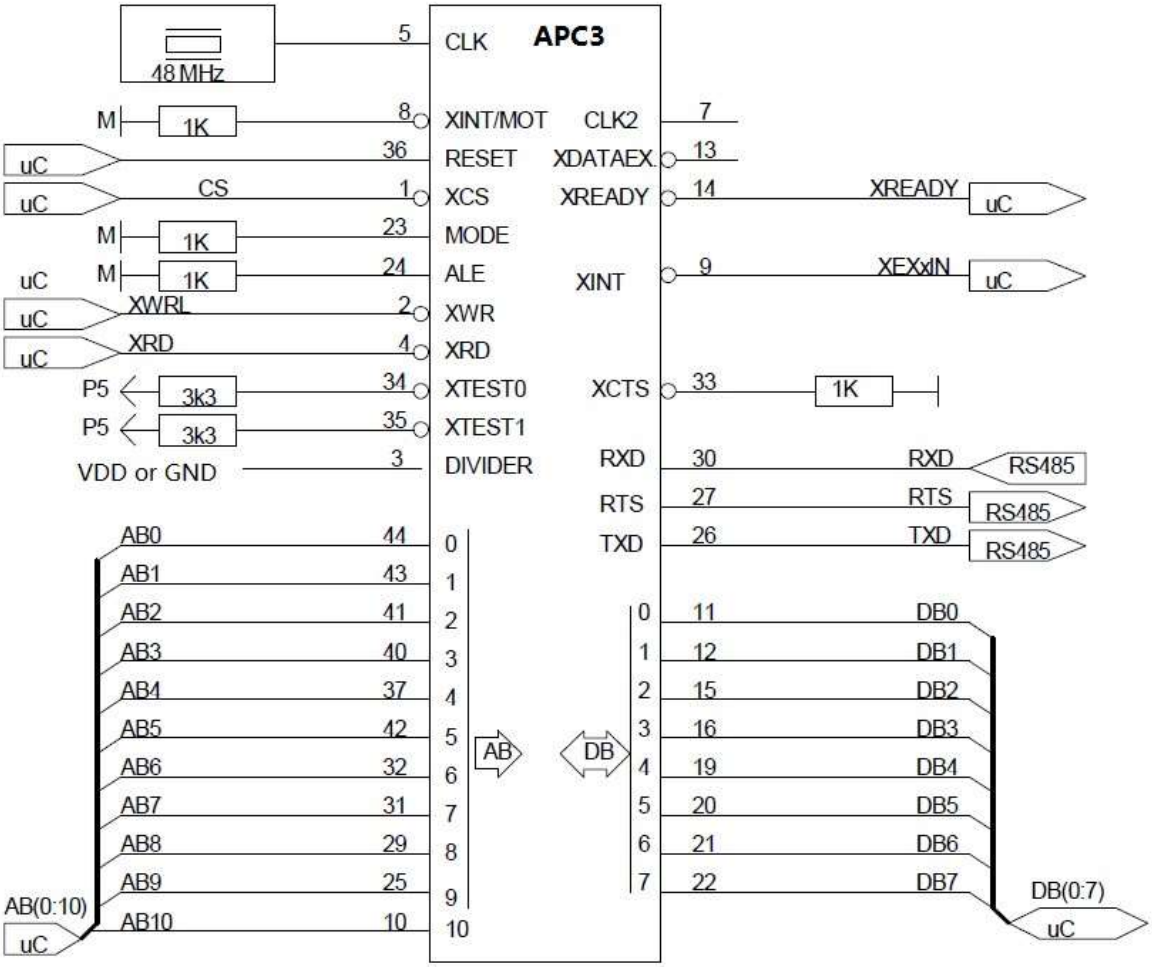

Figure 6.6 80C165 Application

The pull-up/pull-down resistor in the above figure is only available on the circuit tester.

Chapter 7. Packaging information

APC3 is packaged by PQFP-44.

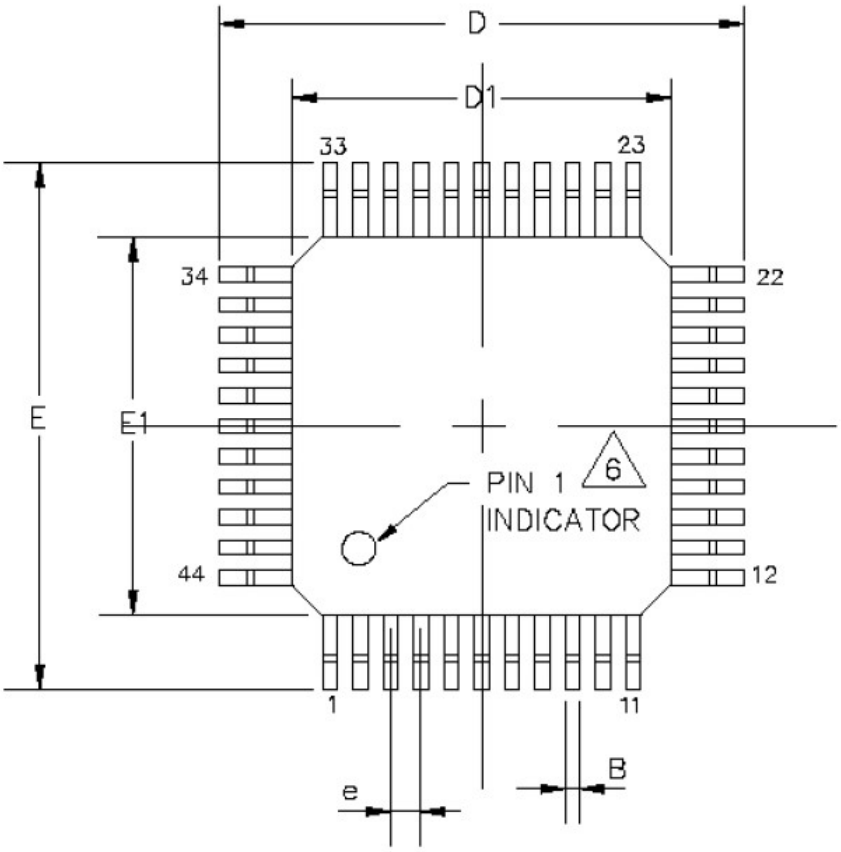

Figure 7.1 Package Drawing

Appendix A Some DPV0 service formats

A.1 Set_Slave_Address（SAP55）

Table A.1 Set_Slave_Address service structure

Byte	Bit Position								Designation
	7	6	5	4	3	2	1	0	
0									New_Slave_Address
1									Ident_Number_High
2									Ident_Number_Low
3									No_Add_Chg
4-243									Rem_Slave_Data additional application-specific data

Note：

- Byte 0： new address given
- Byte 1：ID_High
- Byte 2：ID_Low
- Byte 3： Allow address modification flag. 0: The address can be further modified; 1: The address cannot be further modified.
- Whether the slave address can be modified can be set in the GSD file:

Set_Slave_Add_supp=0，the address cannot be modified

Set_Slave_Add_supp=1，the address cannot be modified

A.2 Set_Param (SAP61)

Table A.2 Set_Param Service Structure

Byte	Bit Position								Designation
	7	6	5	4	3	2	1	0	
0	Lock	Unlock	Sync	Free	WD	Res	Res	Res	Station status
1									WD_Fact_1
2									WD_Fact_2
3									MinTSDR
4									Ident_Number_High
5									Ident_Number_Low
6									Group_Ident
7	0	0	0	0	0	WD_	Dis	Dis	Spec_User_Prm_Byte
8-243									User_Prm_Data

Byte7			
Bit	Name	Significance	Default State
0	Dis_Startbit	The start bit monitoring in the receiver is switched off with this bit.	Dis_Startbit= 1 , that is, start bit monitoring is switched off.
1	Dis_Stopbit	Stop bit monitoring in the receiver is switched off with this bit	Dis_Stopbit= 0, that is, stop bit monitoring is not switched off.
2	WD_Base	This bit specifies the time base used to clock the watchdog. WD_Base = 0: time base 10 ms	WD_Base= 0, that is, the time base is 10 ms
3-7		0	0

Note：

- Byte1/2 is used to calculate the watchdog timing time. The watchdog function enables the slave station to continuously monitor the activity of the master station during the communication process. Once the master station is found to be abnormal and has not recovered to normal after exceeding the watchdog time TWD, it will enter the protection state. The setting of TWD is independent of the communication rate, and this function is activated by Bit3 in Byte0.
- TWD = WD_Fact_1×WD_Fact_2×10ms(10ms is the basic unit for calculating time)
- minTSDR is an important indicator reflecting the real-time performance of the slave station. It means that the slave must pass the time specified by minTSDR before responding to the request of the master. Here, minTSDR takes Tbit as the unit. Tbit is the transmission time of 1-bit, which is equal to the reciprocal of the communication rate. MinTSDR defaults to 11Tbit. If it is 0, minTSDR remains unchanged. The user needs to save the minTSDR parameter in EEPROM.
- The ID information represented by Byte4/5 must be consistent with the Ident of the slave station_ The number must be consistent with the Ident in the GSD file_ The number information is consistent.
- Group number information in Byte6 is used to cooperate with DDLM_ Global_ Control service, in which 8 bits define 8 groups respectively. This group number and DDLM_ Global_ The group numbers in the Control message match to determine which slave stations need to respond to the DDLM_ Global_ Command in Control message.

A.3 Check_Config（SAP62）

Generally, slave stations are composed of Slot as the basic logical unit. A slot can be regarded as a module. Modules correspond to physical I/O function points, such as digital or analog I/O modules. Empty Slots are represented by empty modules.

DP slave station generally has two structures:

1. Fixed module structure: composed of one or more constant modules.
2. Variable module structure: the slave station includes a group of modules from which one or more modules can be selected to form the actual slave station structure during configuration.

There are two formats for the definition of modules, as follows:

1. Complete format

   Each module corresponds to a defined bytecode. The input and output data of up to 16 bytes or word length in this module can be described by bytes, as shown in the following table.

Table A.3 Complete format structure definition

Bit7	Bit6	Bit5	Bit4	Bit3 Bit2 Bit1 Bit0	Description
		0	1	0~15	Exchange data length, 0~15 means 1~16
		x	0		
		0 0 1	0 1 0		Special format (described later) Input Output
	0				Byte structure
	1				Word structure
0					The data of a single byte or word is consistent
1					The data of the whole module is consistent

Note：

- A module defined in a complete format can contain 1~16 bytes or word data
- Consistency refers to whether a single byte or word can represent a single data, or whether multiple bytes or words in the front and back need to represent a data together.
- Example: 0x13 represents a 4-byte input module; 0x23 indicates a 4-byte output module.

2. Special format

Use multiple bytes or words to define a module. In this way, data of 64 bytes or words can be described. at most. See the following table for specific definitions:

Table A.4 Special format structure definition

Bit7	Bit6	Bit5	Bit4	Bit3 Bit2 Bit1 Bit0	Description
		0	0		Special header format

				0~15	Data length specified by manufacturer 0=empty
0	0				Empty position
0	1				Followed by a byte representing the length
1	0				Followed by a byte representing the length
1	1				Followed by a byte representing the length

The structure of bytes representing the length is defined in the following table:

Table A.5 Structure definition of bytes representing length

Bit7	Bit6	Bit5 Bit4 Bit3 Bit2 Bit1 Bit0	Description
		0~63	Input/output data length 00=1 byte or word
	0		Byte structure
	1		Character structure
0			The data of a single byte or word is consistent
1			The data of the whole module is consistent

Example:

Byte No.	Bit Position								Designation
	7	6	5	4	3	2	1	0	
1	1	1	0	0	0	0	1	1	input/output,
2	1	1	0	0	1	1	1	1	consistency, output, 16 words
3	1	1	0	0	0	1	1	1	consistency, input, 8 words
4	Manufacturer Specific data								
5									
6									

Note：

In a special format, the manufacturer can add more information. For example, the slave station supports two types of 16 bit input modules with different functions, so different contents can be added to the module description information to distinguish between the two modules.

A.4 Slave_Diagnosis (SAP60)

The first six bytes in the diagnostic information are standard information, reflecting the working status of the slave station, and their values are automatically generated by the APC3 chip. The following describes the standard data definitions in diagnostic information.

Bytes1：Station_status_1

Table A.6 Standard data definition in diagnostic information

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
							x(M)	Station_Non_Existent (It means that the slave station does not exist, and
						x		Station_Not_Ready (1 indicates that the slave station is not ready for data exchange)
					x			Cfg_Fault (1 indicates that the configuration parameters
				x				Ext_Diag (A value of 1 indicates that the standard diagnostic information is followed by the extended diagnostic information)
			x					Not_Supported (1 means that the slave station does not support
		x						Invalid_Slave_Response (1 means the slave response is invalid)

	x							Prm_Fault （1 indicates the last Set_Prm message error)
x(M)								Master_Lock (1 means that the slave station is locked by another

Note：

- x (M) indicates that this bit is set by the master station, and this bit is set as 0 by the slave station.

Byte2: Station_status_2

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
							x	Prm_Req (1 means that the slave station must be re
						x		Stat_Diag (static diagnostics) (If it is 1, the master station needs to repeatedly diagnose the slave station, and the true bit is 0)
					1			1
				x				WD_On (Watchdog on) (If it is 1, the watchdog function will be activated)
			x					Freeze_Mode (Set 1 after the slave station receives the
		x						Sync_Mode (Set 1 after the slave station receives the
	0							0
X(M)								Deactivated

Note：

- x (M) indicates that this bit is set by the master station, and this bit is set as 0 by the slave station.

Byte3: Station_status_3

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
	0	0	0	0	0	0	0	reserved
x								Ext_Diag_Overflow (There is too much diagnostic information. If the diagnostic

Byte4: Master_Add

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
0~125（0x00~0x7E）								Master station address

Note：

- Set the slave station_ The primary station address for Prm operation. The default value is 255 (0xFF).

Byte5/6: Ident_Number

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
0~255（0x00~0xFF）								Ident_Number high byte
0~255（0x00~0xFF）								Ident_Number low byte

Current Station_ status_ Ext in 1_ When the Diag position is 1, there will be extended diagnostic information starting from the 7th byte, which involves device related or user specified diagnostic information. The specific information is divided into the following three categories, and the specific definitions will not be introduced here:

- Device related diagnostic information
- Diagnostic information related to the module
- Diagnostic information related to the channel

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